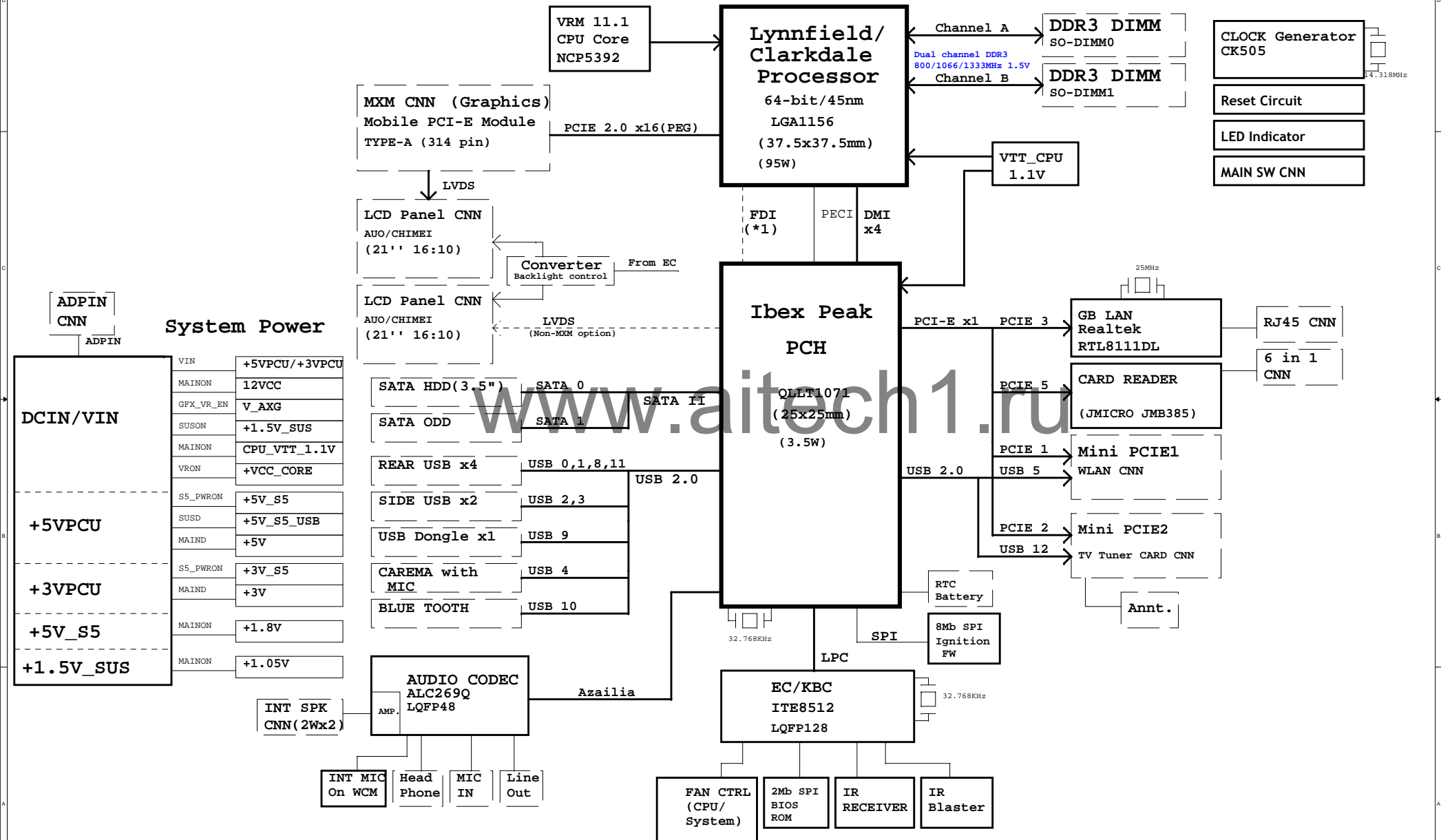


Schematic Page Description :

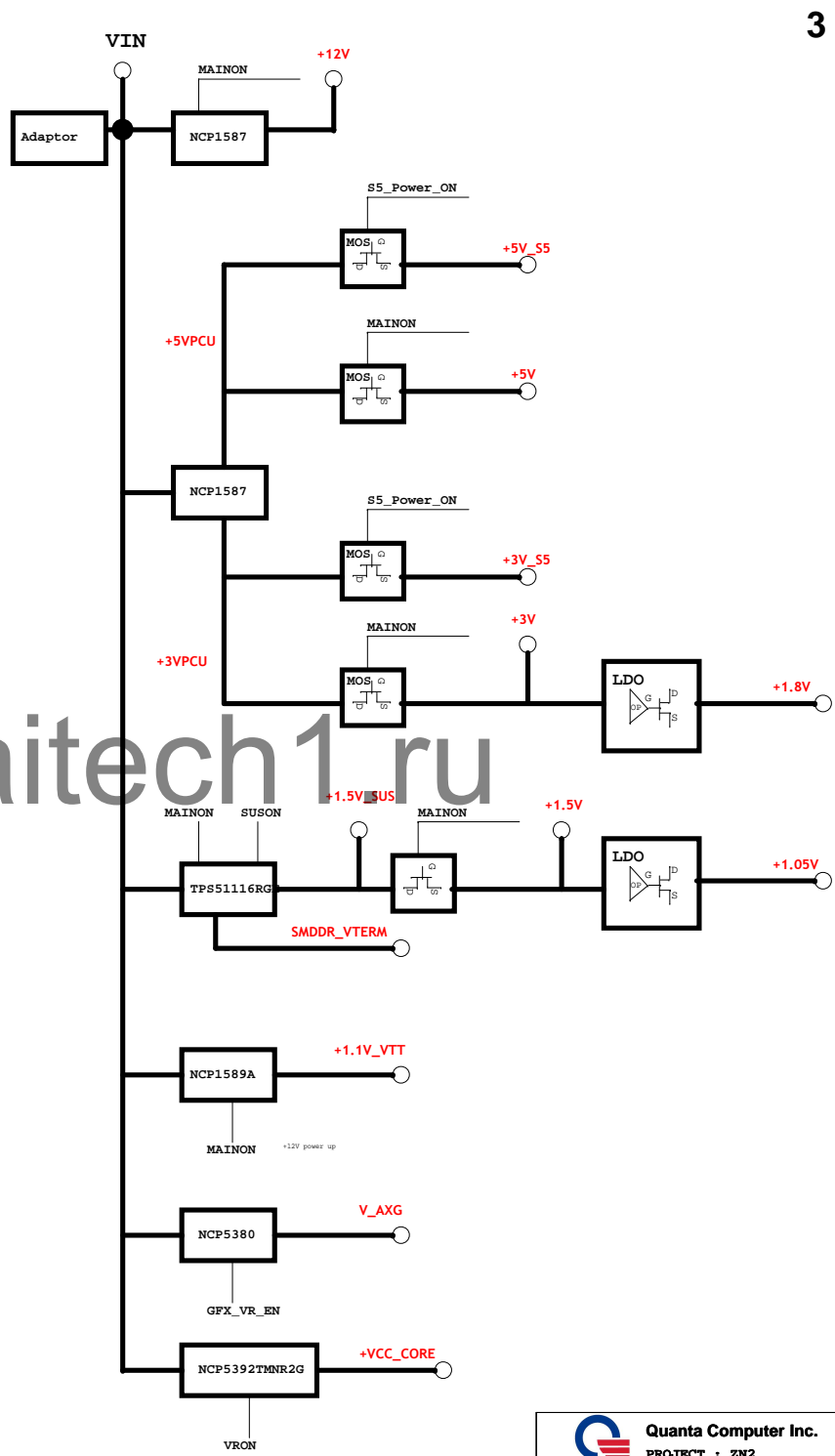
01 -- Page Description	19 -- PCH 1/6 (DMI/FDI/VIDEO)	39 -- ADP AC IN & HDD12V
02 -- System Block Diagram	20 -- PCH 2/6(SATA/RTC/HDA/LPC)	41 -- V_AXG (ISL6314)
03 -- Power Map	21 -- PCH 3/6(PCIE/USB/CLK/NV)	42 -- DDR3 1.5V(TPS51116)
04 -- Power Sequence 1/2	22 -- PCH 4/6(GPIO/CPU)	43 -- CPU_VTT(ISL6314CRZ)
05 -- Power Sequence 2/2	23 -- PCH 5/6(POWER)	44 -- CPU_CORE (NCP5392)
06 -- Clock	24 -- PCH 6/6(GND)	45 --1.05V_PCH, 1.05V_ME,1.8V
07 -- SMBus Block Diagram	25 -- MXM 3.0	46 -- Discharge Circuit
08 -- GPIO list	26 --AUDIO CODEC ALC269	47 -- CHANGE LIST1
09 -- CLOCK GENERATOR	27 --LINE OUT/CRT	48 -- CHANGE LIST2
10 -- MCP 1/7(CLK/CTRL/MISC)	28 --JMB380 (Card Reader/1394)	49 -- ANNOTATIONS
11 -- MCP 2/7(DDR3 CHANNEL A)	29 -- SATA HDD/ODD	
12 -- MCP 3/7(DDR3 CHANNEL B)	30 --MINI PCIE(WLAN/TV/IR/BT)	
13 -- MCP 4/7(PCIE/DMI)	31 --ON BOARD USB	
14 -- MCP 5/7(VCCP)	32 --LCD PANEL/INVERTER	
15 -- MCP 6/7(MISC/VCC)	33 --LAN(RTL8111DL)	
16 -- MCP 7/7(GND)	34 --LAN Transformer & RJ45	
17 -- DDR3 CHA DIMM0	35 --FAN/D board/CCD/PS2	
18 -- DDR3 CHB DIMM0	36 -- EC ITE 8512N/FLASH	
	37 -- XDP	
	38 -- SCREW HOLE	

Block Diagram :

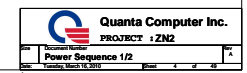


(*1)FDI - Used only for the Clarkdale processor.

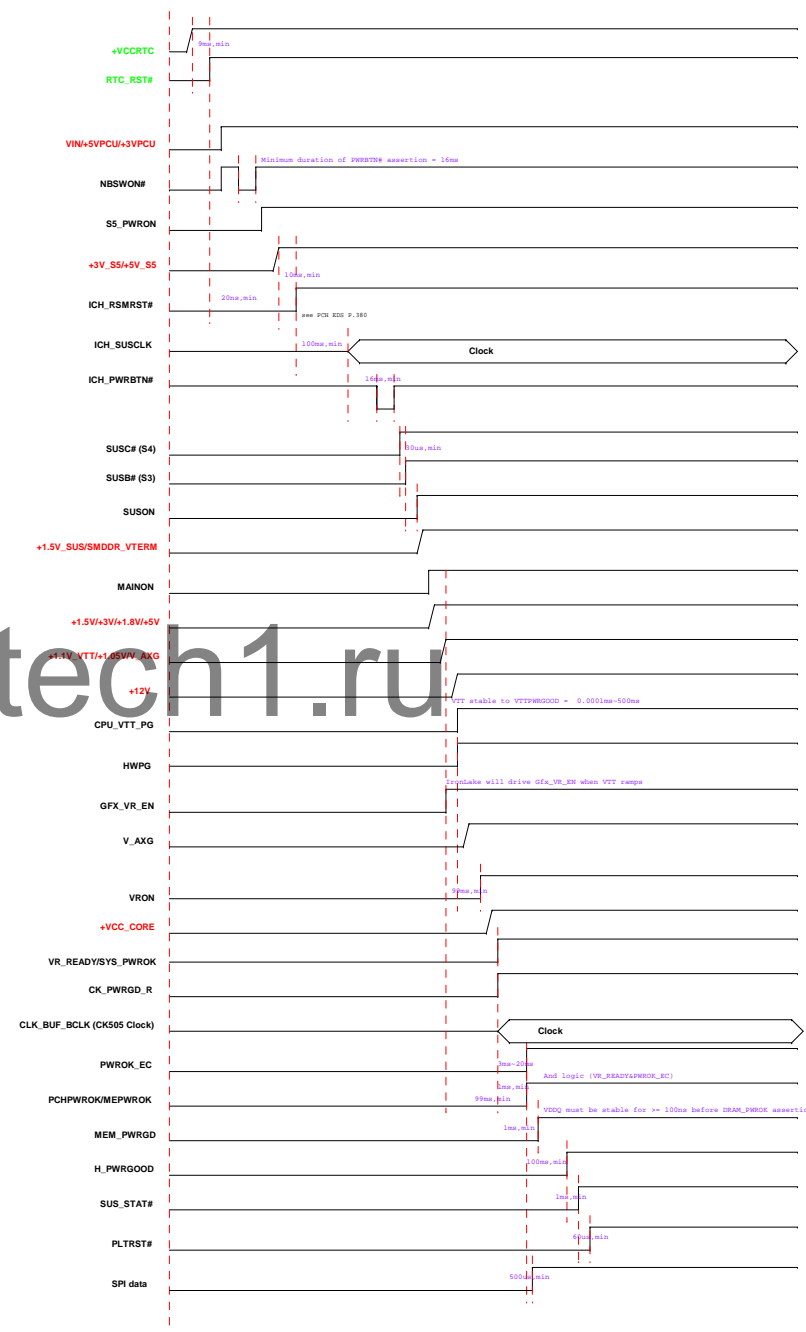
Power Rail	Destination	Voltage	SO Current
+VCC_CORE	Lynnfield : Default for initial power up	0.65V-1.4V 1.1V	90A(TDC)
V_AXG	for 92W TDP SKU for 79W TDP SKU	0.5-1.3V	10A (TDC) 16A (TDC)
+1.1V_VTT	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V-1.1V-1.155V 1.1V 1.05V-1.1V-1.16V	30A(TDC) 0.065A 0.001A
+1.8V	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F	1.71V-1.8V-1.89V 1.71V-1.8V-1.89V 1.71V-1.8V-1.89V	1.1A 0.196A 0.156A
+1.5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V-1.5V-1.575V	6A
SMDDR_VTERM	DDRIII Terminator:	0.75V	2A
+1.05V	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power	0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V 0.998V-1.05V-1.1V	1.629A 3.251A 0.065A 0.075A 0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)		
+3V	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CH7308 : LVDD ALC662 : DVDD Mini PCIE : +3.3V(WLAN) CAREMA	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.357A 0.069A
+5V	Ibex Peak : Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) ALC662S : AVDD Touch Screen LCD Panel USB: x 12 ports	4.75V-5V-5.25V 5V	0.001A 6A
MXM_12V HDD_12V			
+3V_S5	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN 82578DM : VDD CLK Gen.CK505 : VDD EC(IT8512) : VSTBY SPI FLASH ROM	3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V	0.086A 0.168A 0.006A
+5V_S5	Ibex Peak : Suspend well Ref. Voltage	4.75V-5V-5.25V	0.001A
	INVERTER : Vin FAN_CPU		
+3VPCU			
+5VPCU			
15VPCU			
VIN			

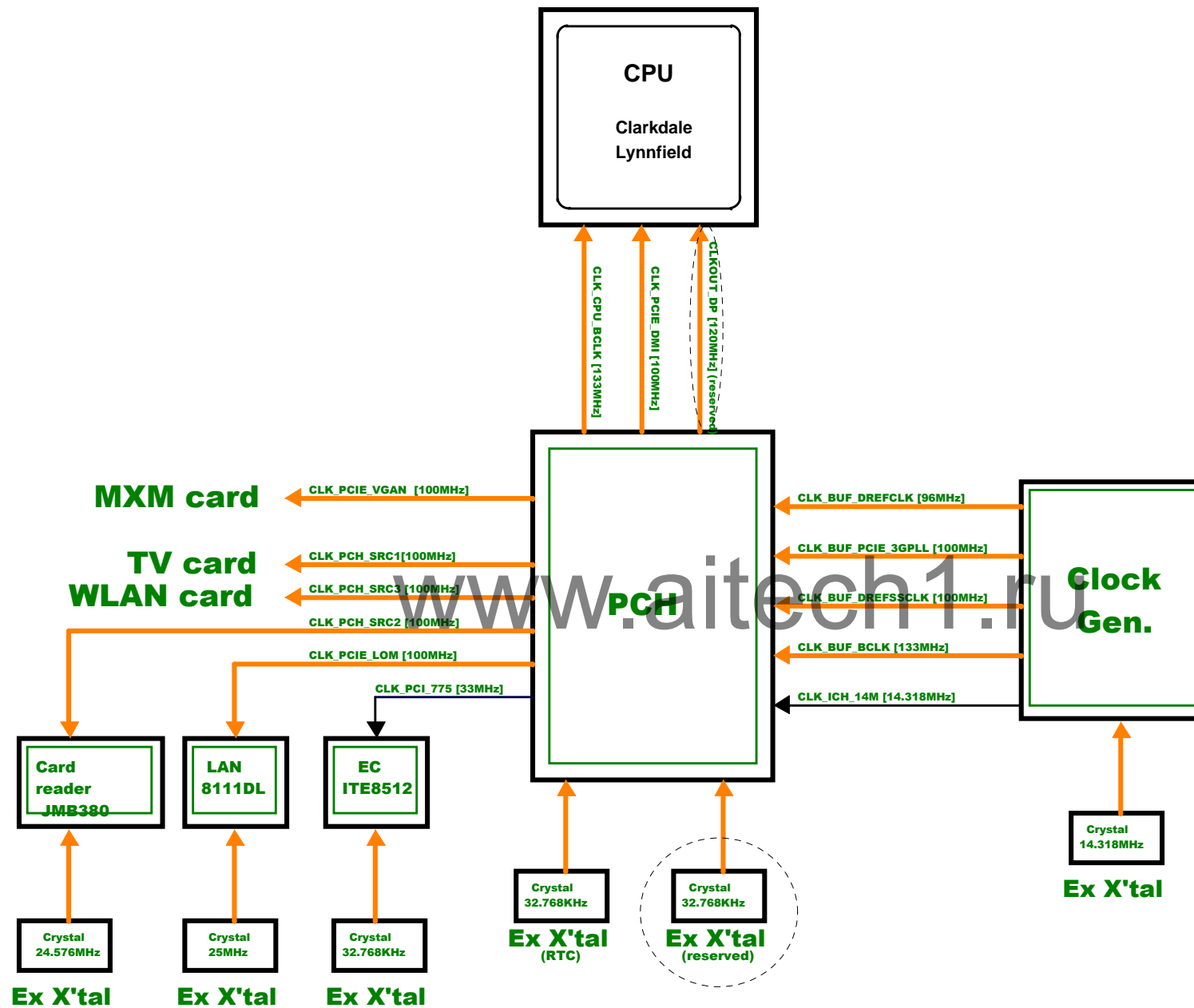


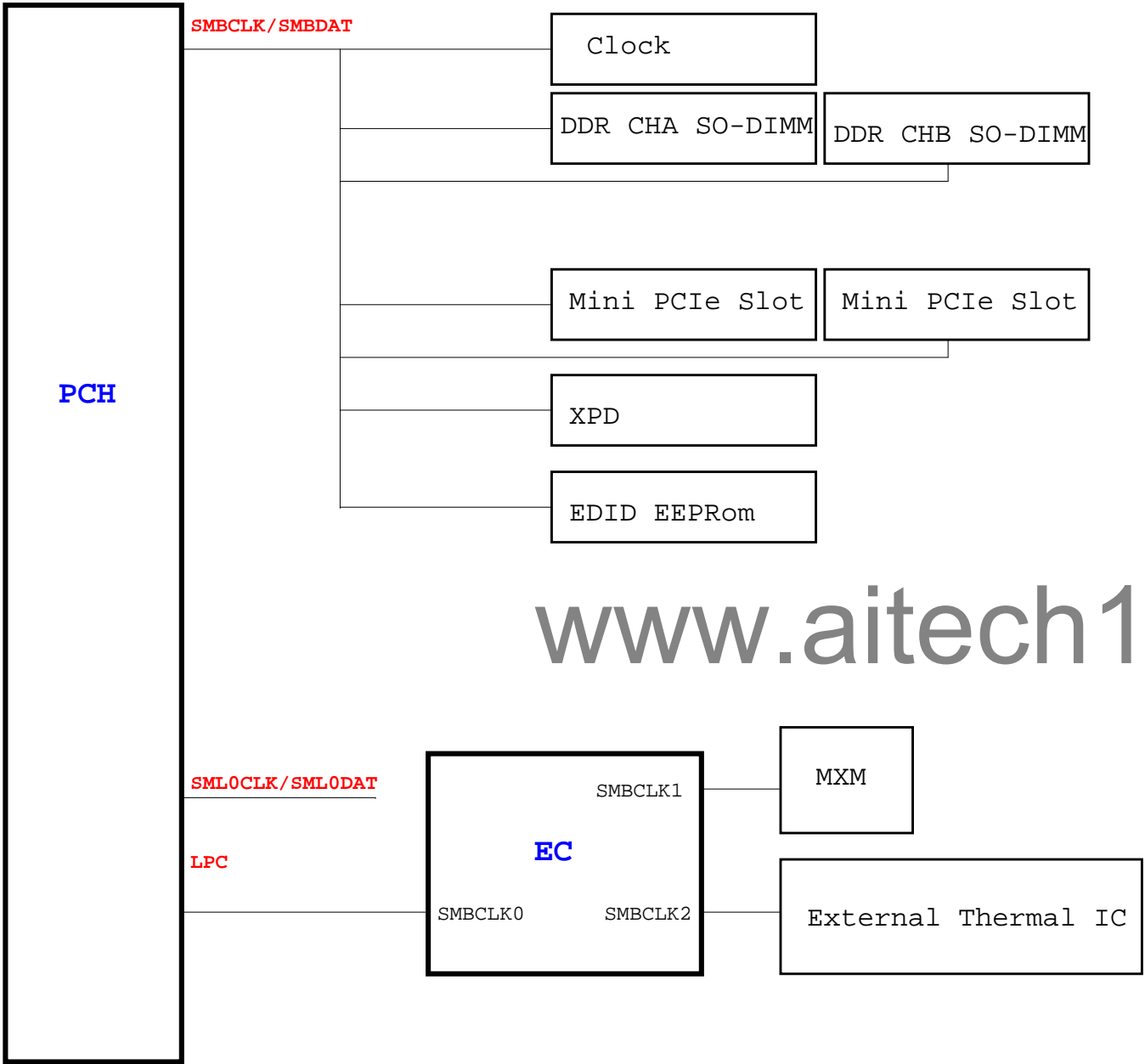
4



Power	Voltage	S0	S3	S4	S5	PCU	G3	Cri Signal
+WCRTC	3V	ON	ON	ON	ON	ON	ON	
VIN	19.5V	ON	ON	ON	ON	ON	OFF	Adaptation
+5VPCU	5V	ON	ON	ON	ON	ON	OFF	Adaptation
+3VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adaptation
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	SS_PWRON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	SS_PWRON
+1.5V_S5S	1.5V	ON	ON	OFF	OFF	OFF	OFF	SUSON
SINCR_VT8000	0.75V	ON	OFF	OFF	OFF	OFF	OFF	SUSON
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.8V	1.8V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
+1.1V_VTT	1.1V/1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON
V_A3IG	777V	ON	OFF	OFF	OFF	OFF	OFF	GFX_VR_EN
+VCC_CORE	777V	ON	OFF	OFF	OFF	OFF	OFF	VRON

[illegible]





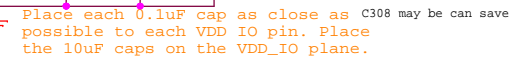
www.aitech1.ru

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITIAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

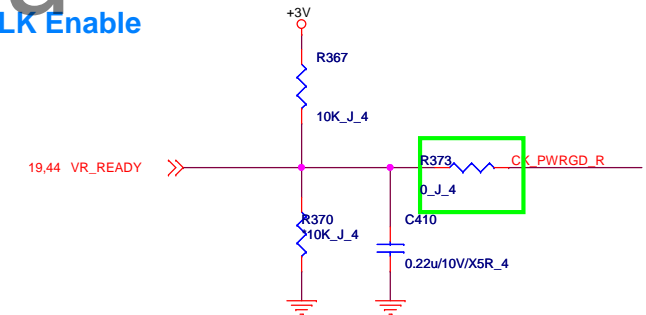
NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		O		
		I		
		I		


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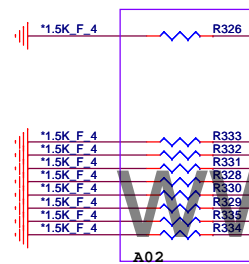
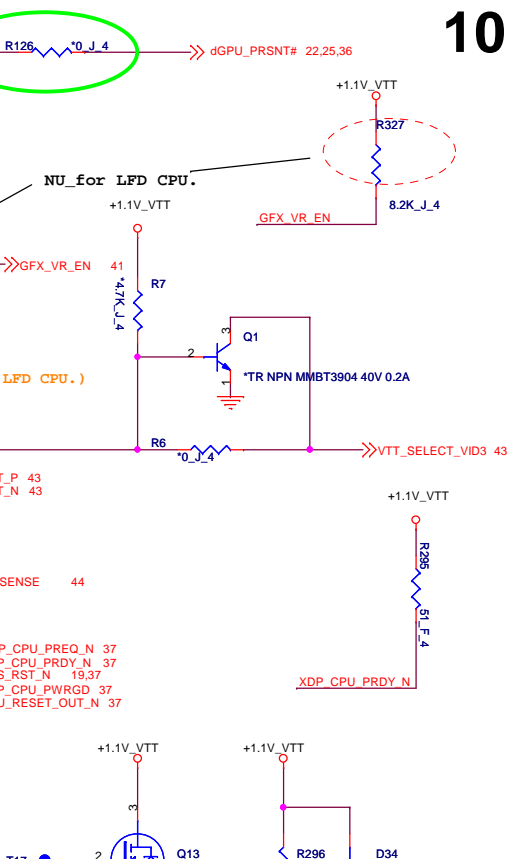
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CLK Enable



 Quanta Computer Inc. PROJECT : ZN2		
Size	Document Number Clock Generator	Rev A
Date: Tuesday, March 16, 2010	Sheet 9 of 49	



CFG 0-6 all internal PULL-UP

21,22,28,30,33 PLTRST#

R282 1K F 4

R291 1.3K F 4

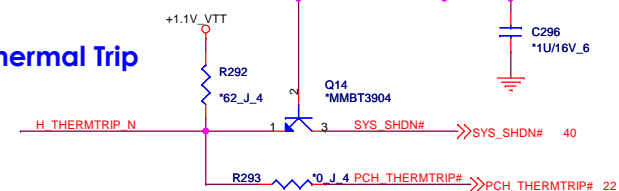
R283 665_F 4

C304 0.1uF/16V/X7R_4

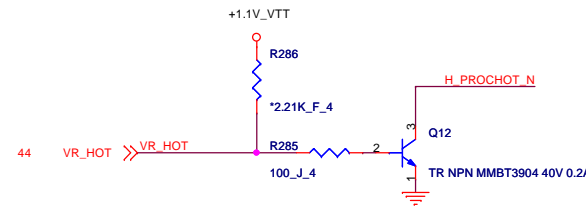
XDP_PFRST_N 37

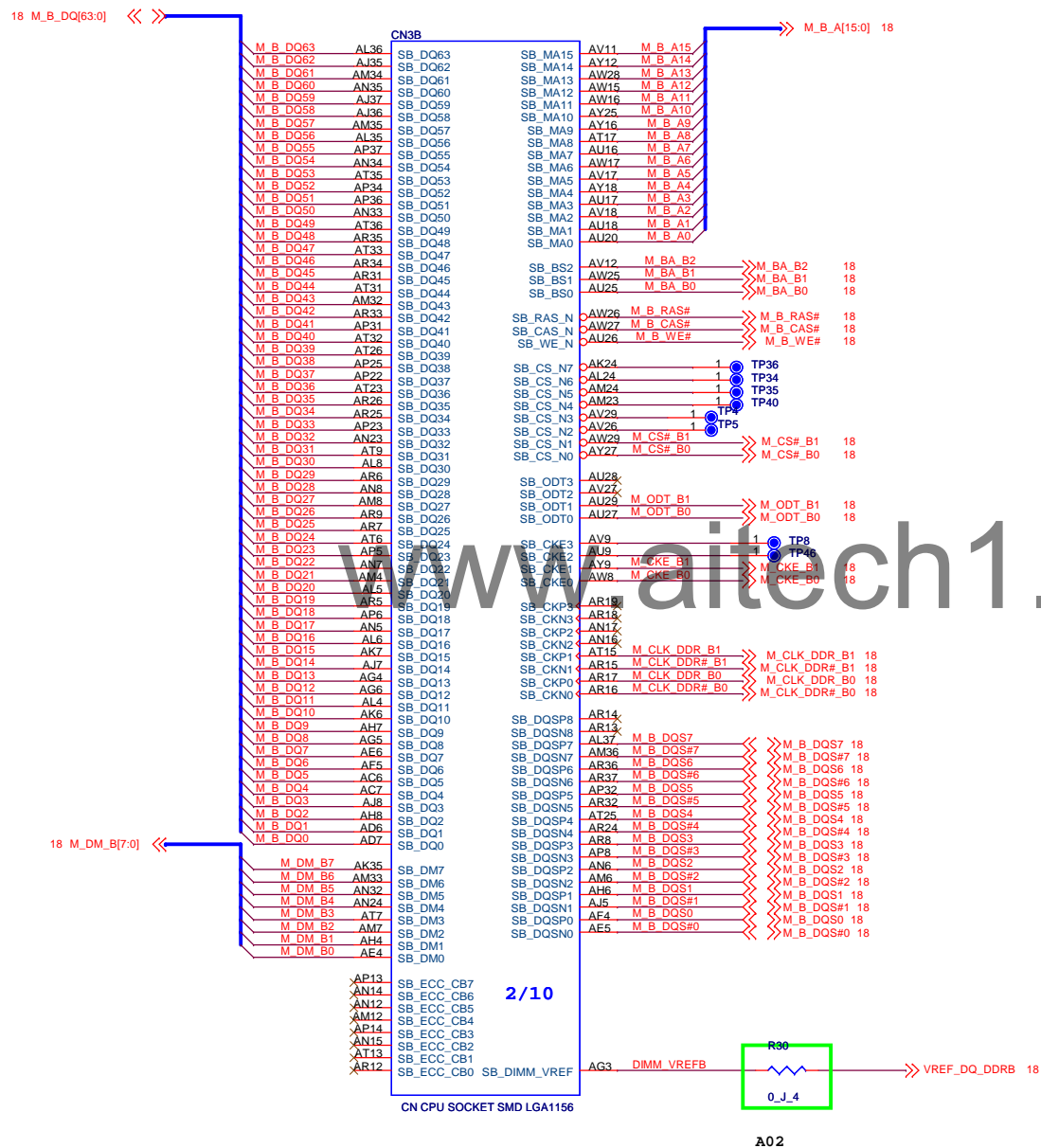
H_CUPRST_N 1.1V level

A02 - PDG1.5 change

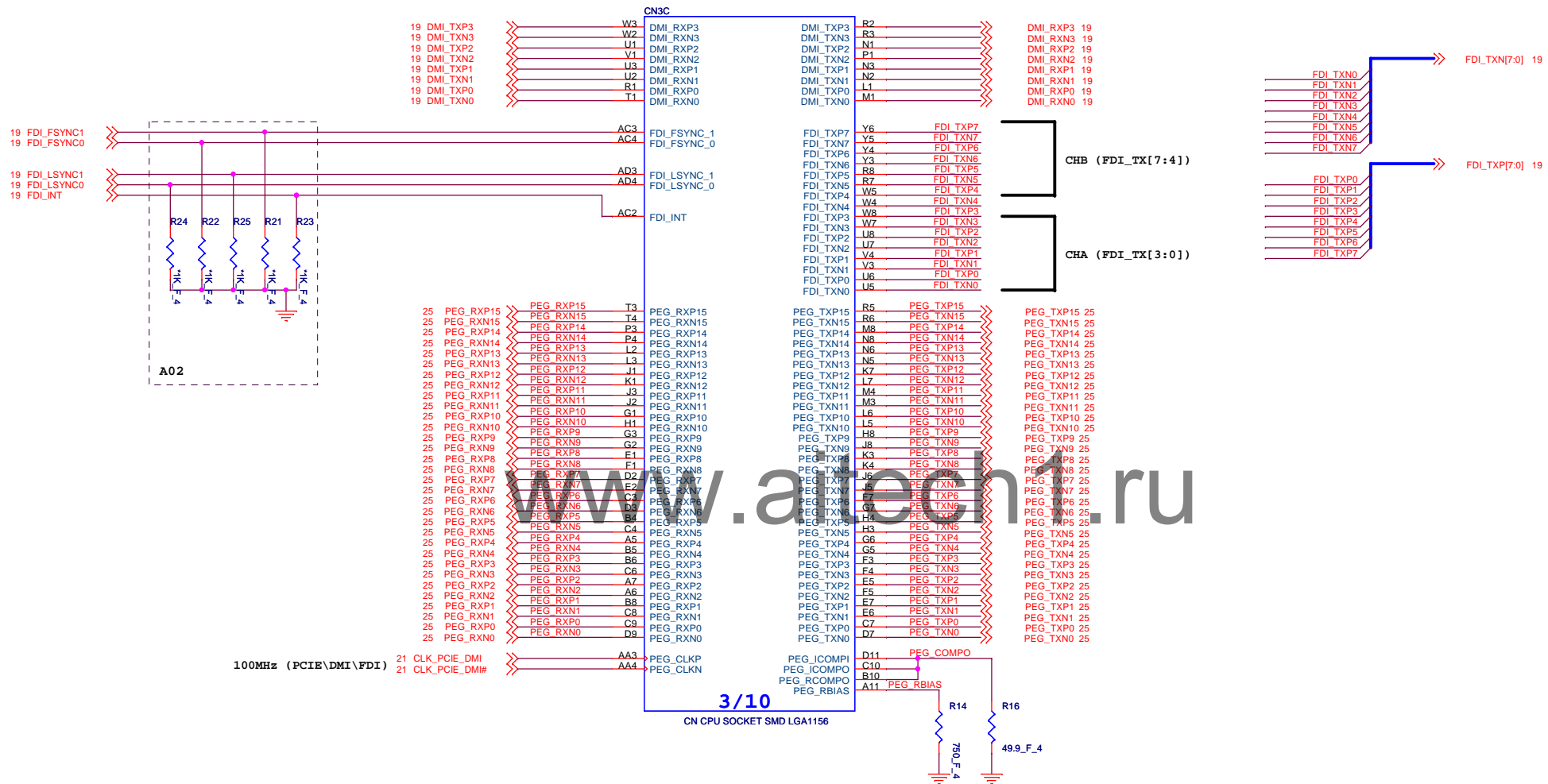


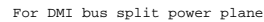
CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU



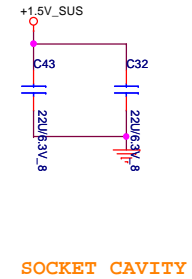
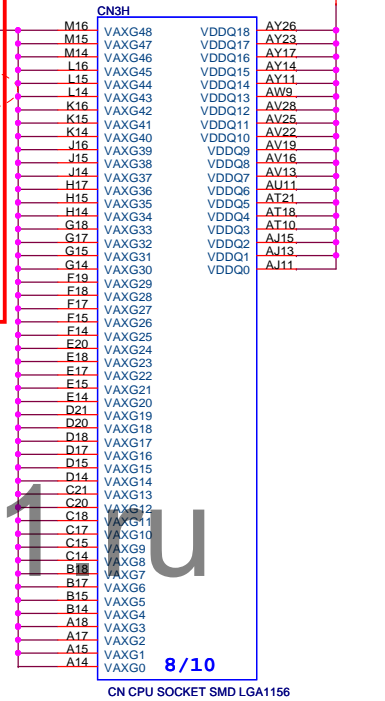
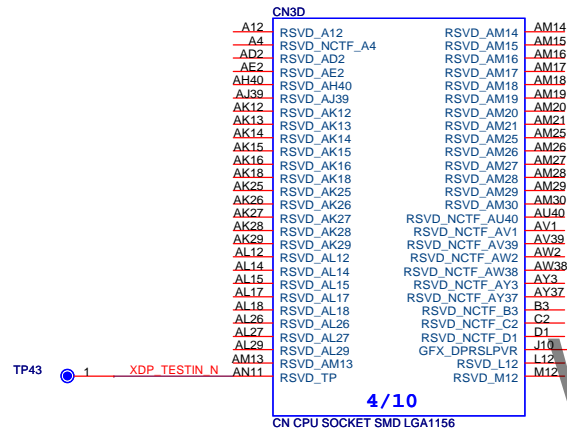
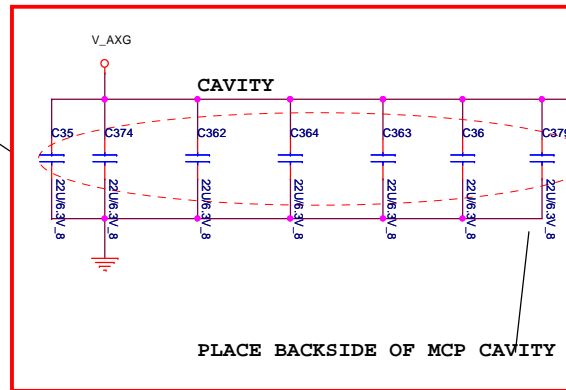


A02





VAXG tie to GND for LFD CPU.



CN3I		
Y7	VSS274	H6
W38	VSS273	H5
W37	VSS272	VSS203
W36	VSS271	VSS202
W35	VSS270	VSS201
W34	VSS269	VSS200
W33	VSS268	VSS199
V5	VSS267	VSS198
U4	VSS266	VSS197
T5	VSS265	VSS196
T38	VSS264	VSS195
T37	VSS263	VSS194
T36	VSS262	VSS193
T33	VSS261	VSS192
R4	VSS260	VSS191
P5	VSS259	VSS190
P2	VSS258	VSS189
N40	VSS257	VSS188
N4	VSS256	VSS187
N37	VSS255	VSS186
N34	VSS254	VSS185
M7	VSS253	VSS184
M6	VSS252	VSS183
M5	VSS251	VSS182
M38	VSS250	VSS181
M35	VSS249	VSS180
M32	VSS248	VSS179
M29	VSS247	VSS178
M26	VSS246	VSS177
M23	VSS245	VSS176
M20	VSS244	VSS175
M2	VSS243	VSS174
M18	VSS242	VSS173
M13	VSS241	VSS172
L9	VSS240	VSS171
L4	VSS239	VSS170
L36	VSS238	VSS169
L33	VSS237	VSS168
L30	VSS236	VSS167
L27	VSS235	VSS166
L24	VSS234	VSS165
L21	VSS233	VSS164
L18	VSS232	VSS163
L13	VSS231	VSS162
K6	VSS230	VSS161
K5	VSS229	VSS160
K40	VSS228	VSS159
K37	VSS227	VSS158
K34	VSS226	VSS157
K31	VSS225	VSS156
K28	VSS224	VSS155
K25	VSS223	VSS154
K22	VSS222	VSS153
K2	VSS221	VSS152
K19	VSS220	VSS151
K13	VSS219	VSS150
K11	VSS218	VSS149
J9	VSS217	VSS148
J7	VSS216	VSS147
J4	VSS215	VSS146
J38	VSS214	VSS145
J35	VSS213	VSS144
J32	VSS212	VSS143
J29	VSS211	VSS142
J26	VSS210	VSS141
J23	VSS209	VSS140
J20	VSS208	VSS139
J17	VSS207	VSS138
J13	VSS206	VSS137
	VSS205	VSS136

9/10
CN CPU SOCKET SMD LGA1156

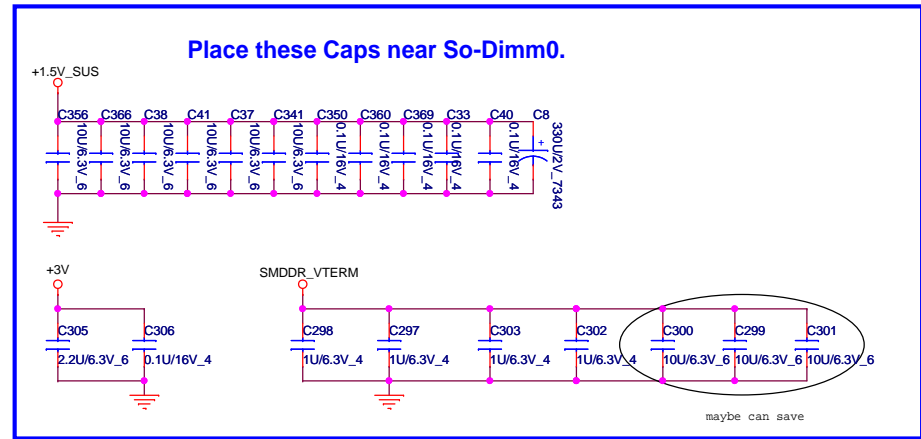
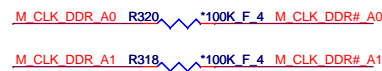
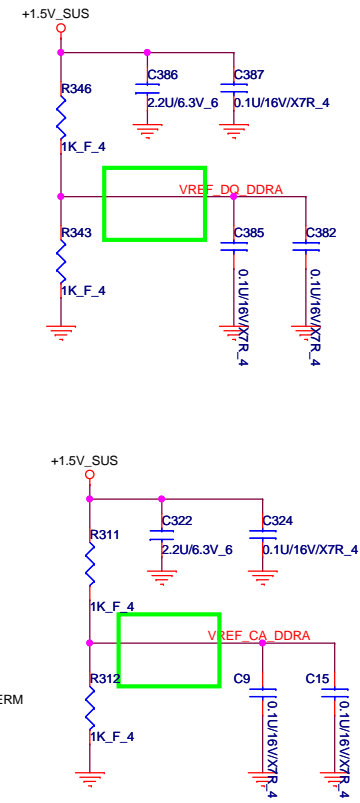
CN3J		
C32	VSS135	VSS68
C29	VSS134	VSS67
C26	VSS133	VSS66
C22	VSS132	VSS65
C19	VSS131	VSS64
C16	VSS130	VSS63
C13	VSS129	VSS62
B8	VSS128	VSS61
B7	VSS127	VSS60
B39	CGC_TP_NCTF	VSS58
B36	VSS126	VSS57
B33	VSS125	VSS56
B30	VSS124	VSS55
B27	VSS123	VSS54
B24	VSS122	VSS53
B16	VSS121	VSS52
AY7	VSS120	VSS52_1
AY4	VSS119	VSS51
AY36	VSS118	VSS50
AY33	VSS117	VSS49
AV38	VSS116	VSS48
AV34	VSS115	VSS47
AV31	VSS114	VSS46
AV3	VSS113	VSS45
AU7	VSS112	VSS44
AU6	VSS111	VSS43
AU36	VSS110_1	VSS42
AU32	VSS110	VSS41
AT8	VSS109_1	VSS40
AT5	VSS109	VSS39
AT37	VSS108	VSS38
AT34	VSS107	VSS37
AT30	VSS106	VSS36
AT27	VSS105	VSS35
AT24	VSS104	VSS34
AT2	VSS103	VSS33
AT16	VSS102	VSS32
AT14	VSS101	VSS31
AT12	VSS100	VSS30
AR40	VSS99	VSS29
AR30	VSS98	VSS28
AR29	VSS97	VSS27
AR20	VSS96	VSS26
AR1	VSS95	VSS25
AP9	VSS94	VSS24
AP7	VSS93	VSS23
AP4	VSS92	VSS22
AP38	VSS91	VSS21
AP35	VSS90	VSS20
AP33	VSS89	VSS19
AP29	VSS88	VSS18
AP27	VSS87	VSS17
AP26	VSS86	VSS16
AP24	VSS85	VSS15
AP20	VSS84	VSS14
AP17	VSS83	VSS13
AP16	VSS82	VSS12
AP15	VSS81	VSS11
AP12	VSS80	VSS10
AN9	VSS79	VSS9
AN4	VSS78	VSS8
AN36	VSS77	VSS7
AN3	VSS76	VSS6
AN31	VSS75	VSS5
AN28	VSS74	VSS4
AN25	VSS73	VSS3
AN22	VSS72	VSS2
AN20	VSS71	VSS1
AN13	VSS70	VSS0
AM9	VSS69	VSS0
	VSS68	VSS0

10/10
CN CPU SOCKET SMD LGA1156

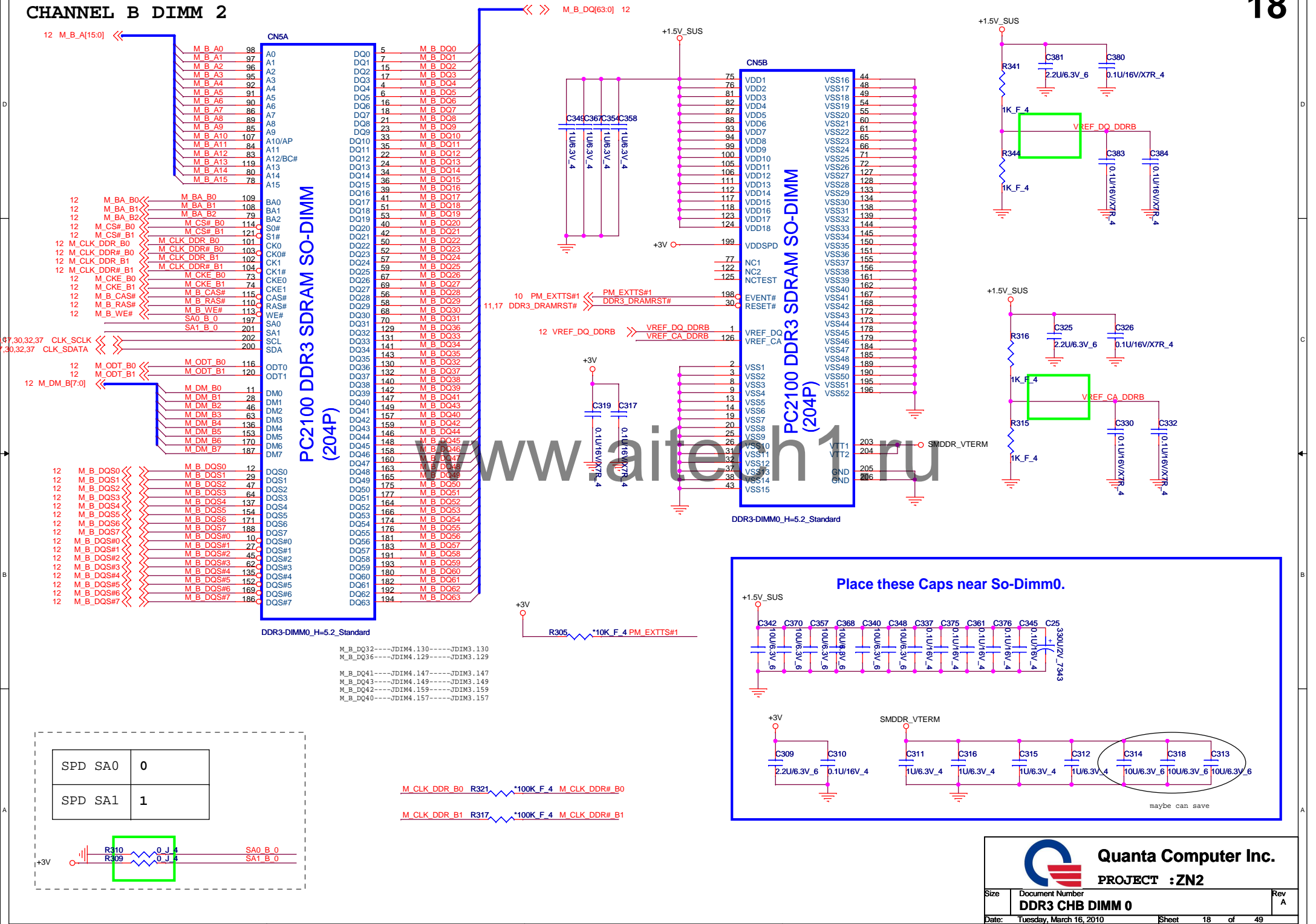


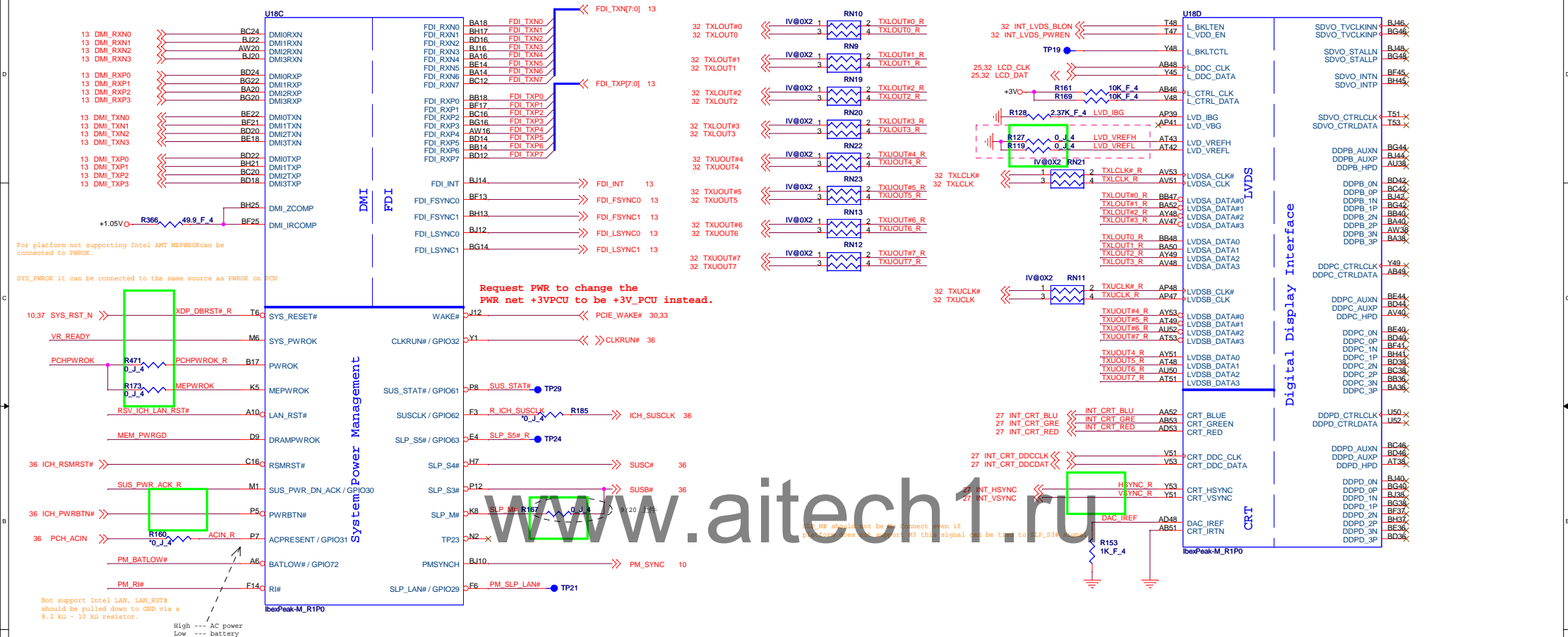
Quanta Computer Inc.
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	MCP (GND)	A
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CHANNEL B DIMM 2



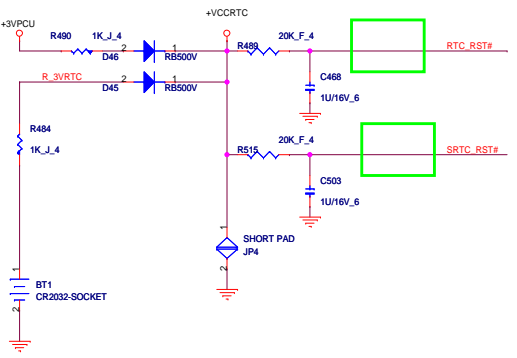


PCH Pull-high/low

DRAMPWROK

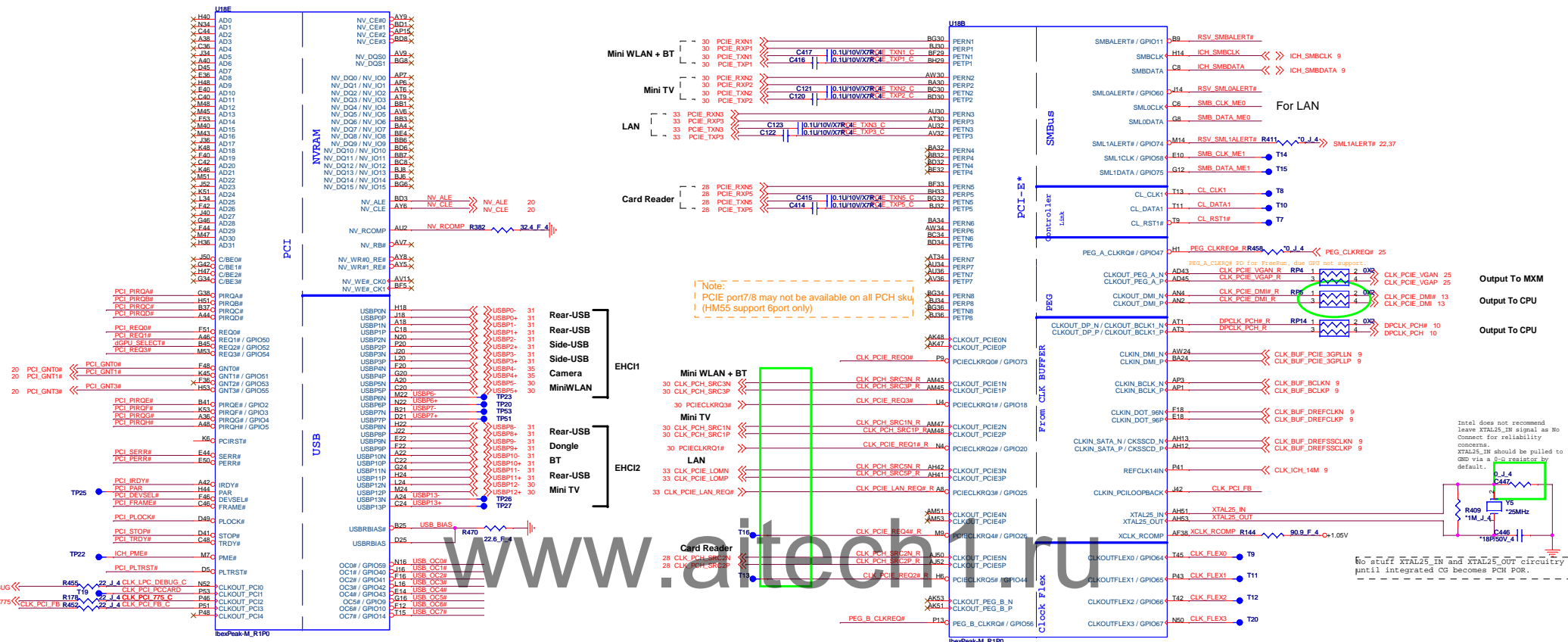
System PWR_OK

RTC Circuitry



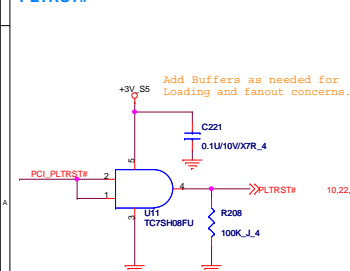
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

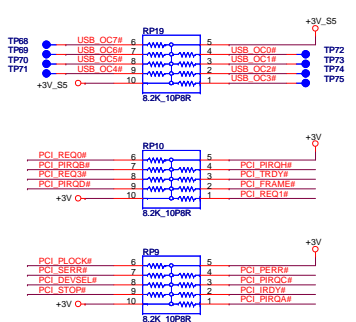


Support PCIe 2.0

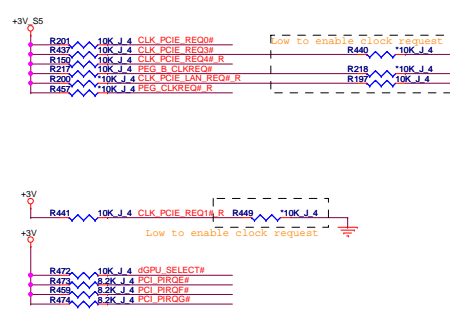
PLTRST#



PCI/USB OC# Pull-up



CLK_REQ/Strap Pin



P20_A_CLKREQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/top-Block Swap Override jumper

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

Boot BIOS Strap

GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

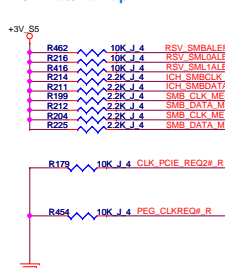
Danbury Technology Enabled

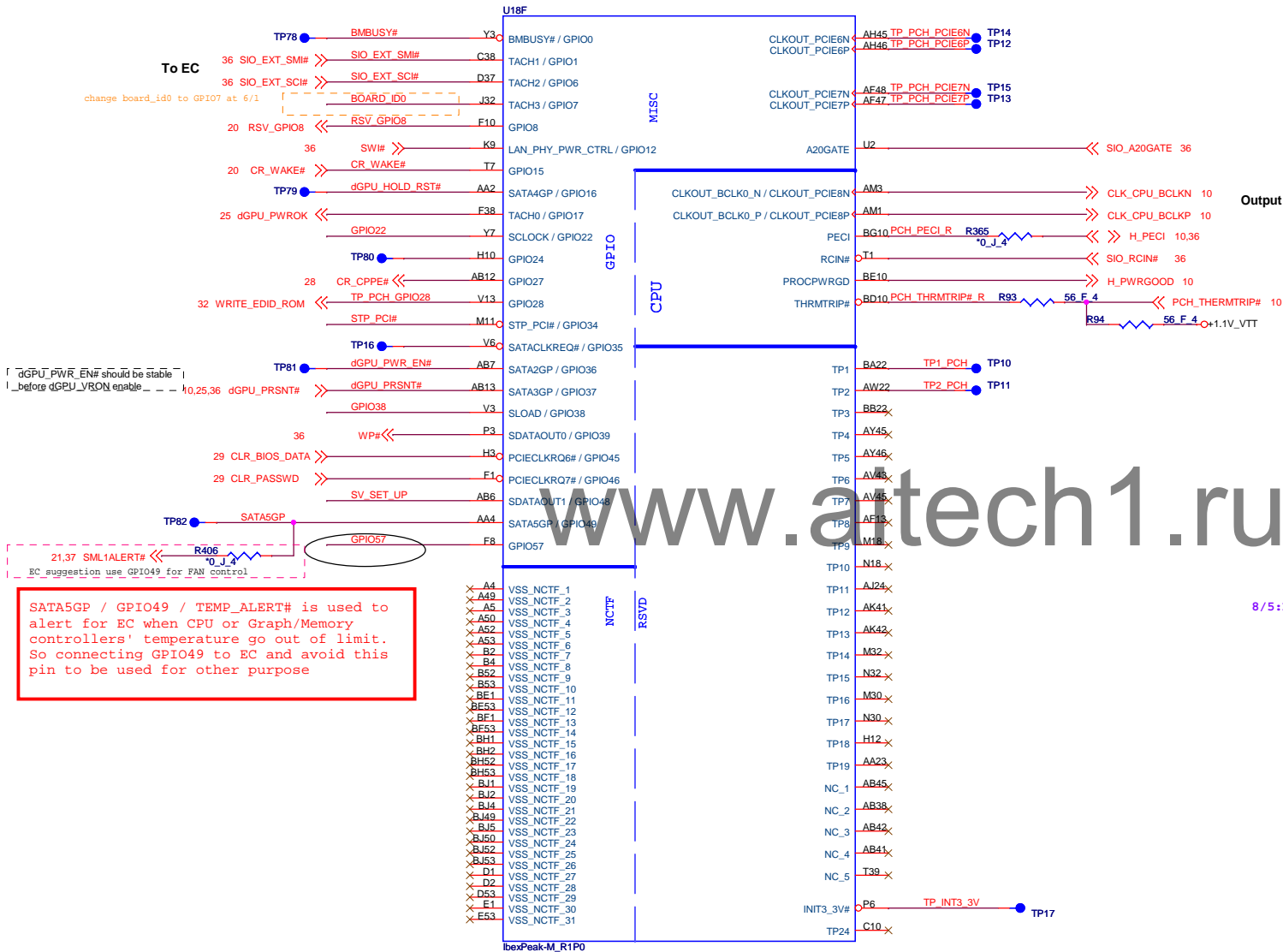
High = Enable
Low = Disable

DMI Termination Voltage

Set to Vcc when LOW
Set to Vcc when HIGH

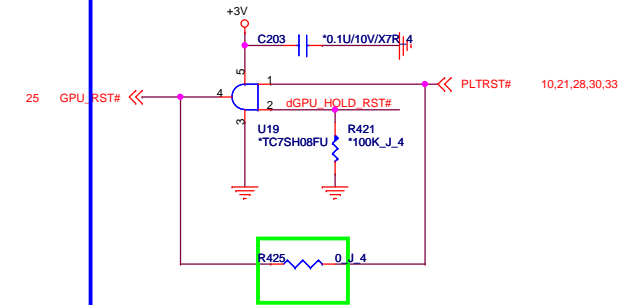
SMBus/Pull-up



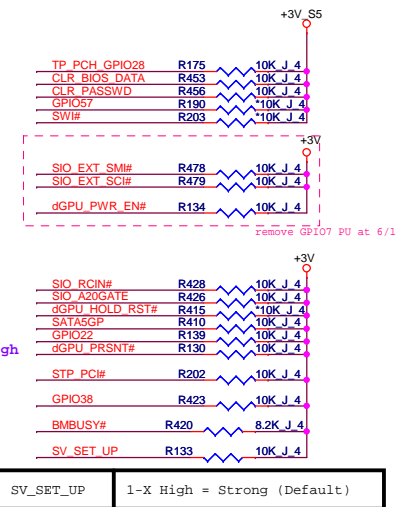


Output To CPU

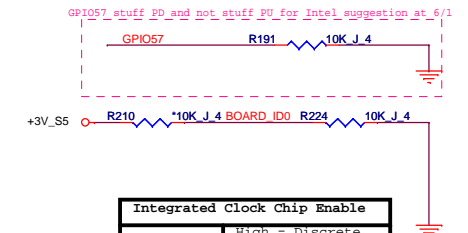
GPU RST#



GPIO Pull-up/Pull-down

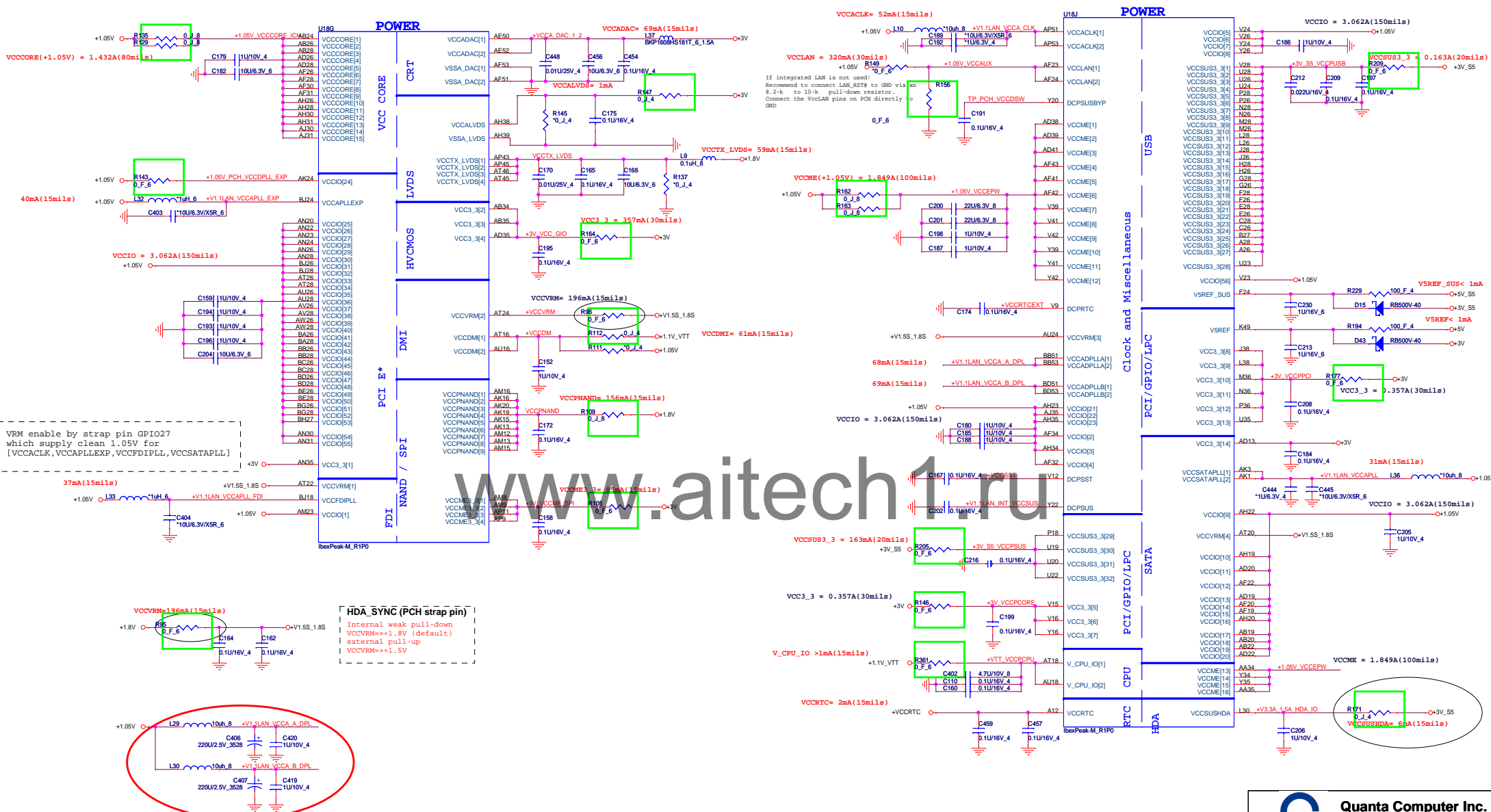


8/5:Default Pull High

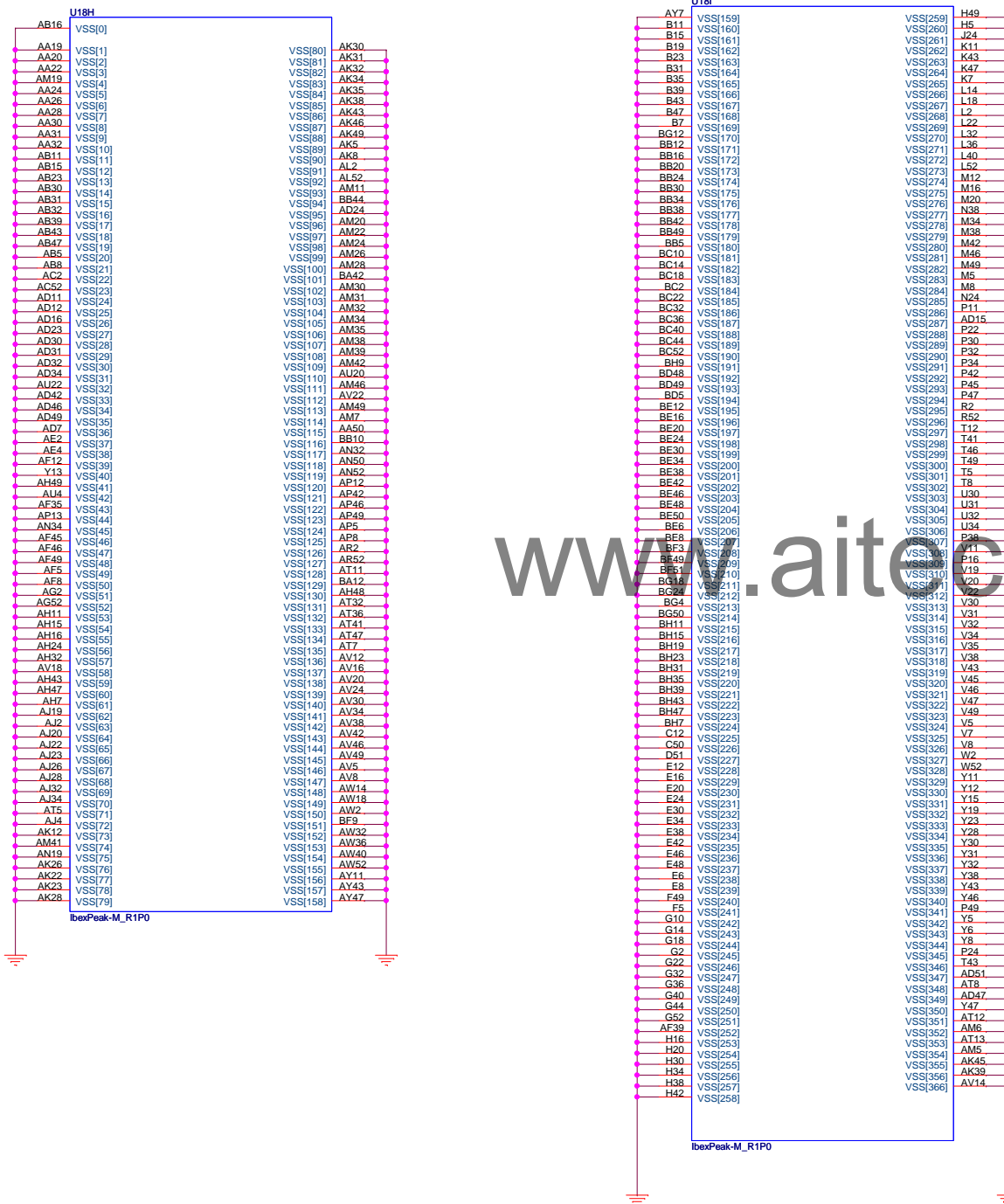


Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)



Quanta Computer Inc.

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625 Change CN22 pin define and footprint at C test.

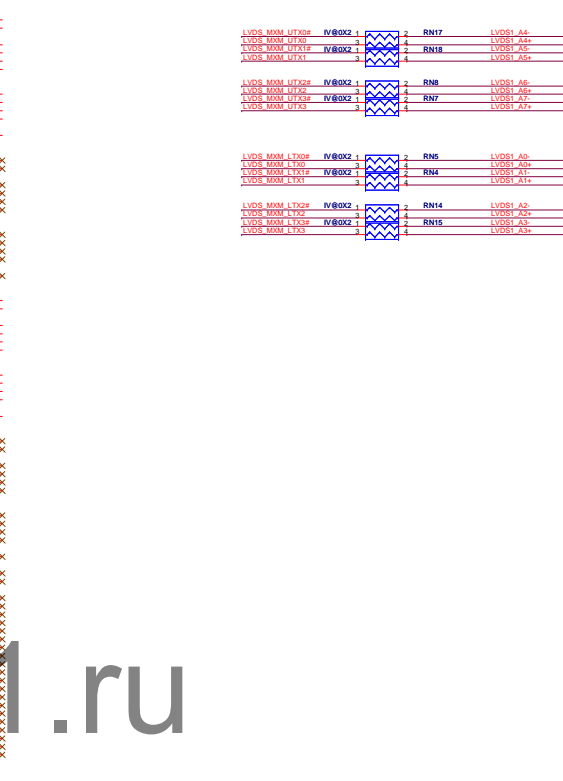
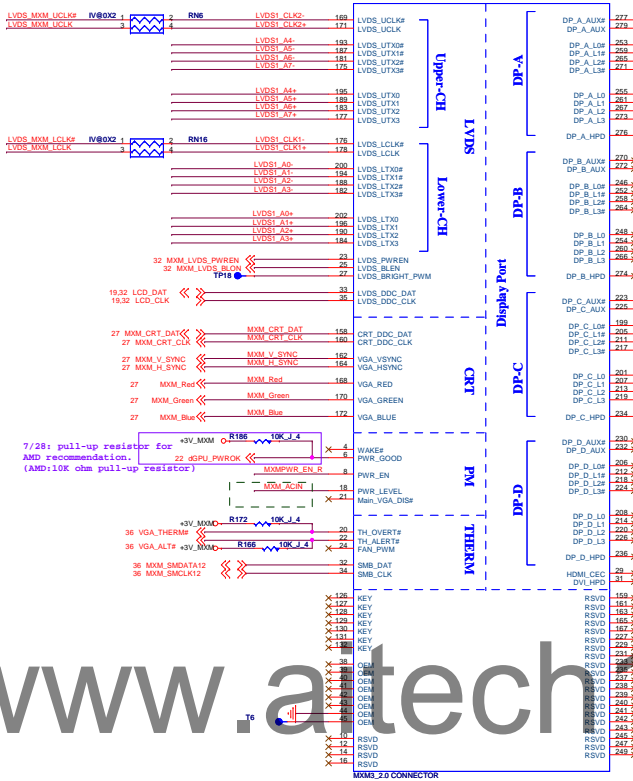
At 11/21
update MXM footprint to mem-mem70-314-31031-1-270p

Check Footprint and P/N

MXM3.0	n-Vidia	AMD
LVDS_D	LVDA	LVDSInt_DP
DP_A	HDMI	HDMI
DP_C	Ext.DP/DVI	Ext.DP/DVI
DP_B	N/A	N/A

dGPU_PSRNT#	Sku
Low	MXM
High	WG/MXM

These capacitors have to be put near to MXM 3.0.



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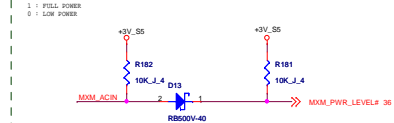
MXM VIN Power switch



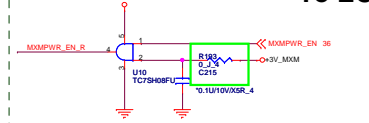
MXM 3V/5V Power switch



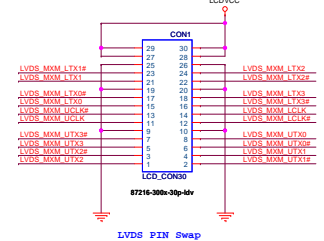
To low power status mode

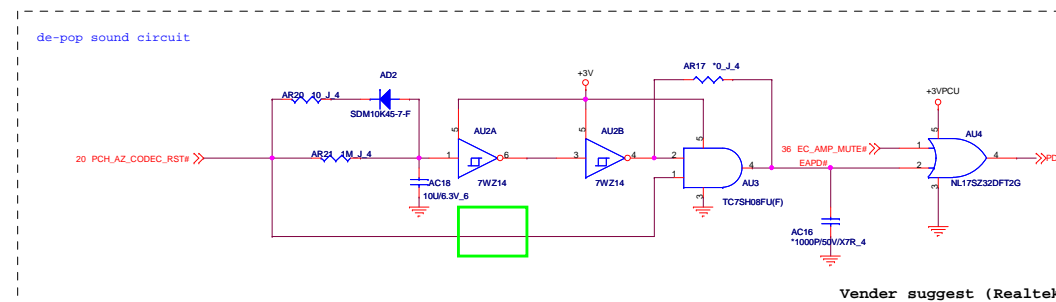
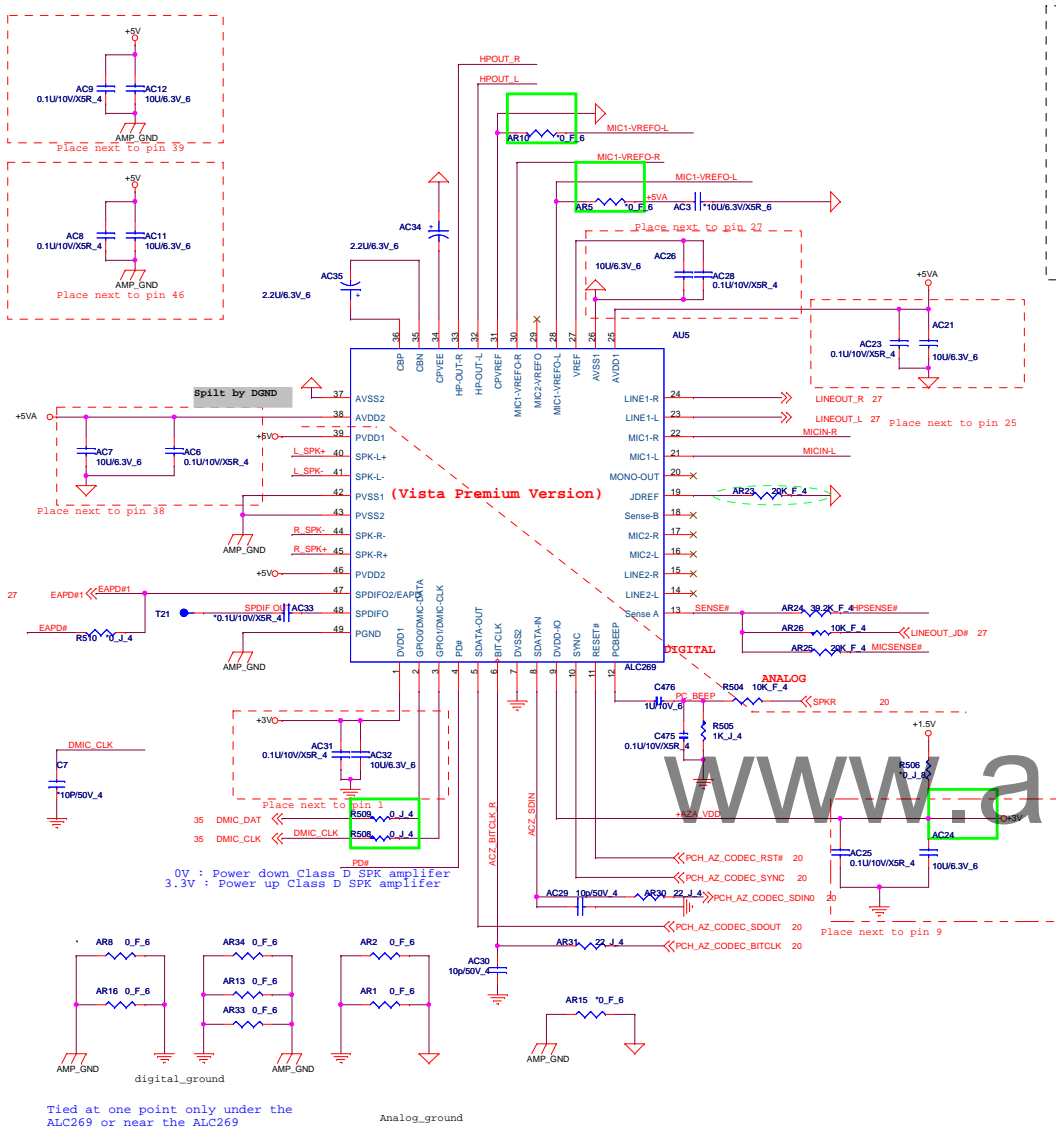


To EC



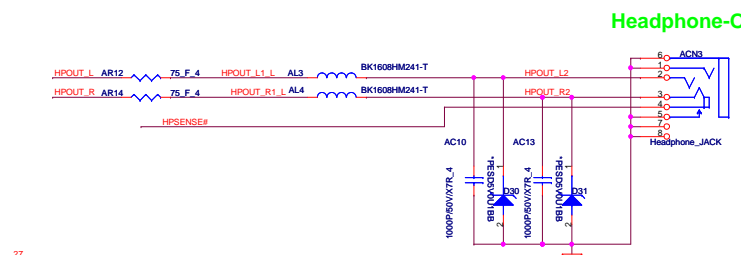
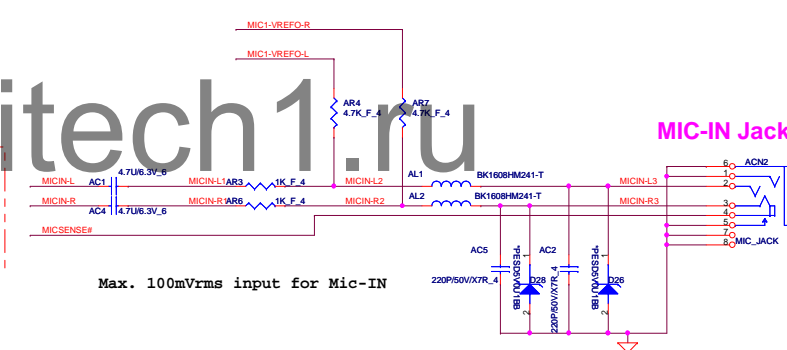
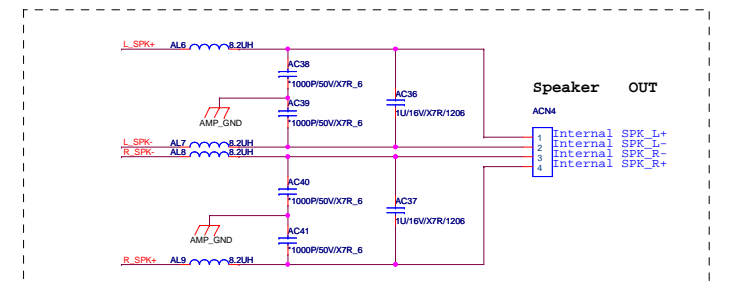
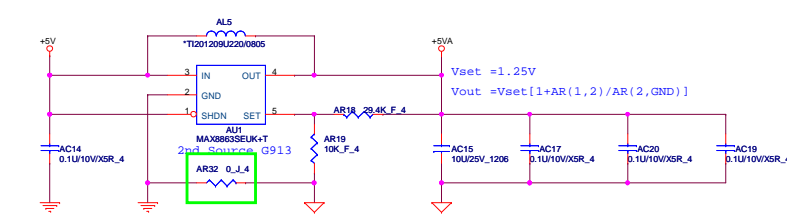
MXM_LVDS_CONNECT

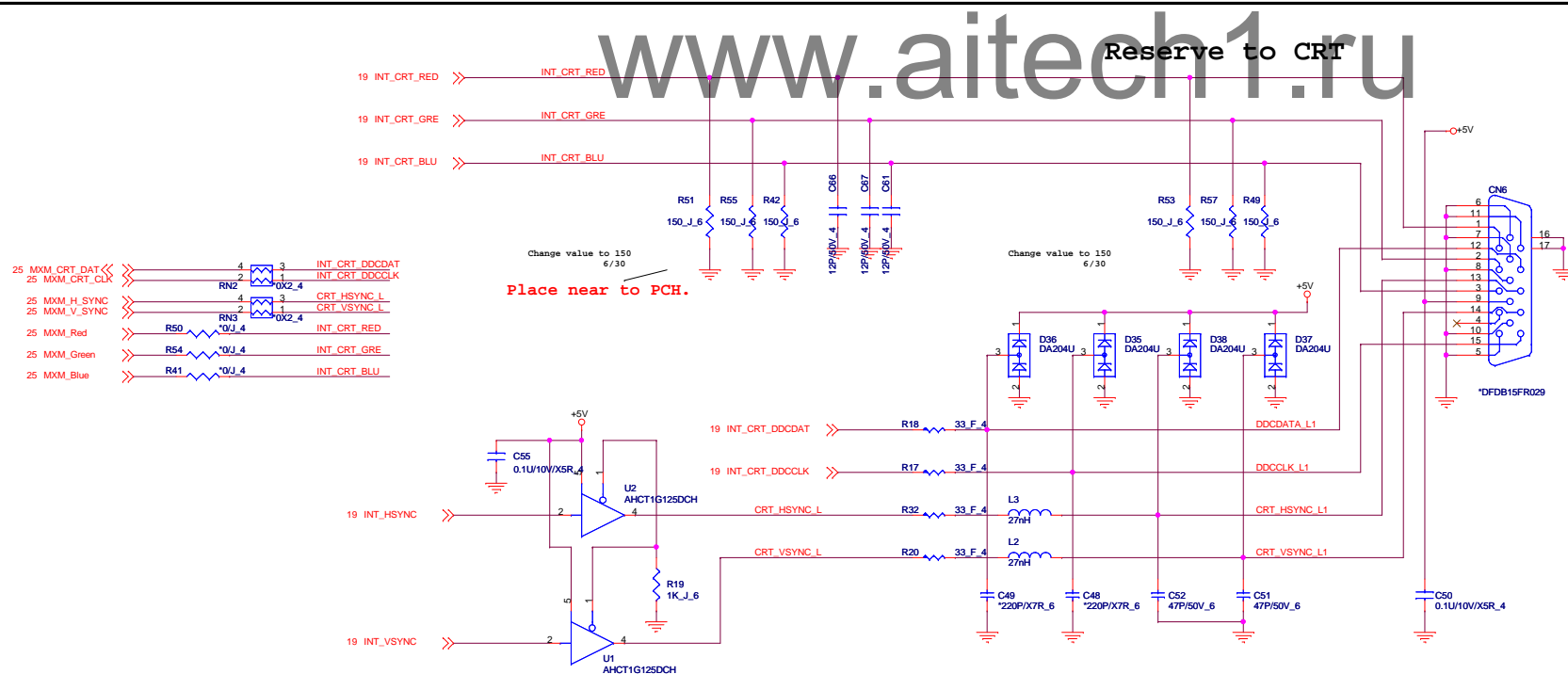
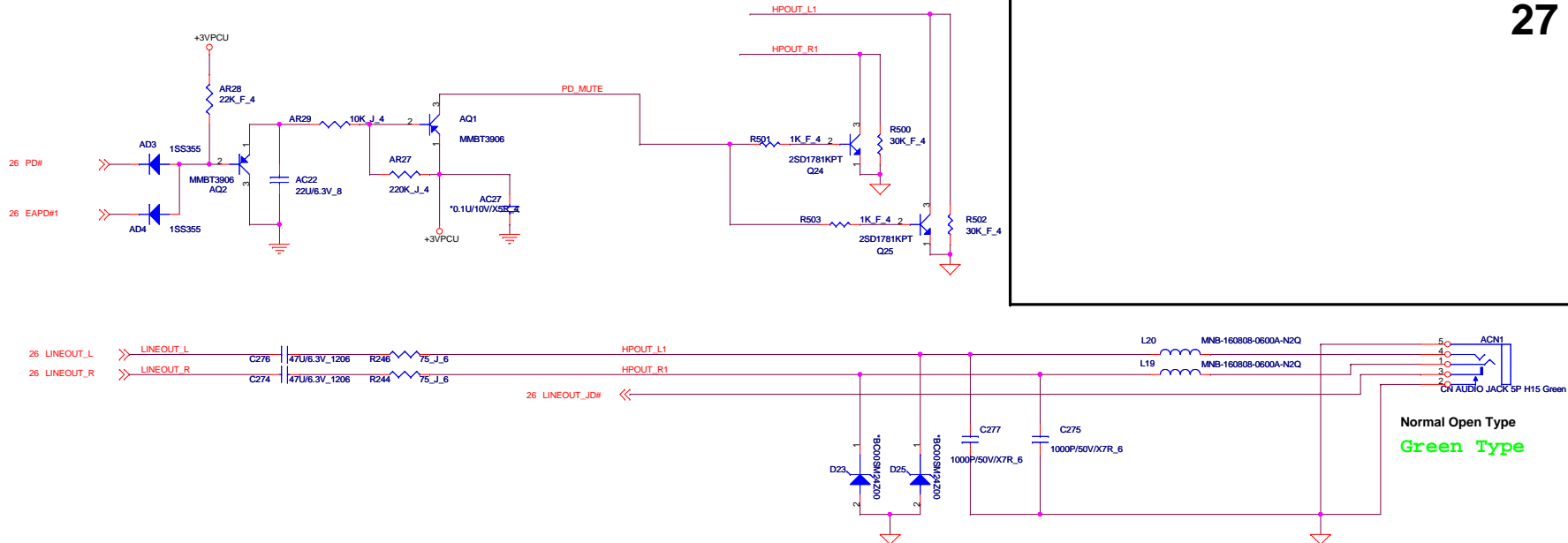


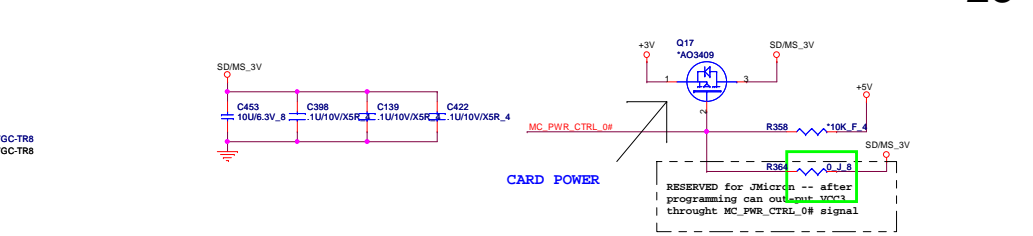
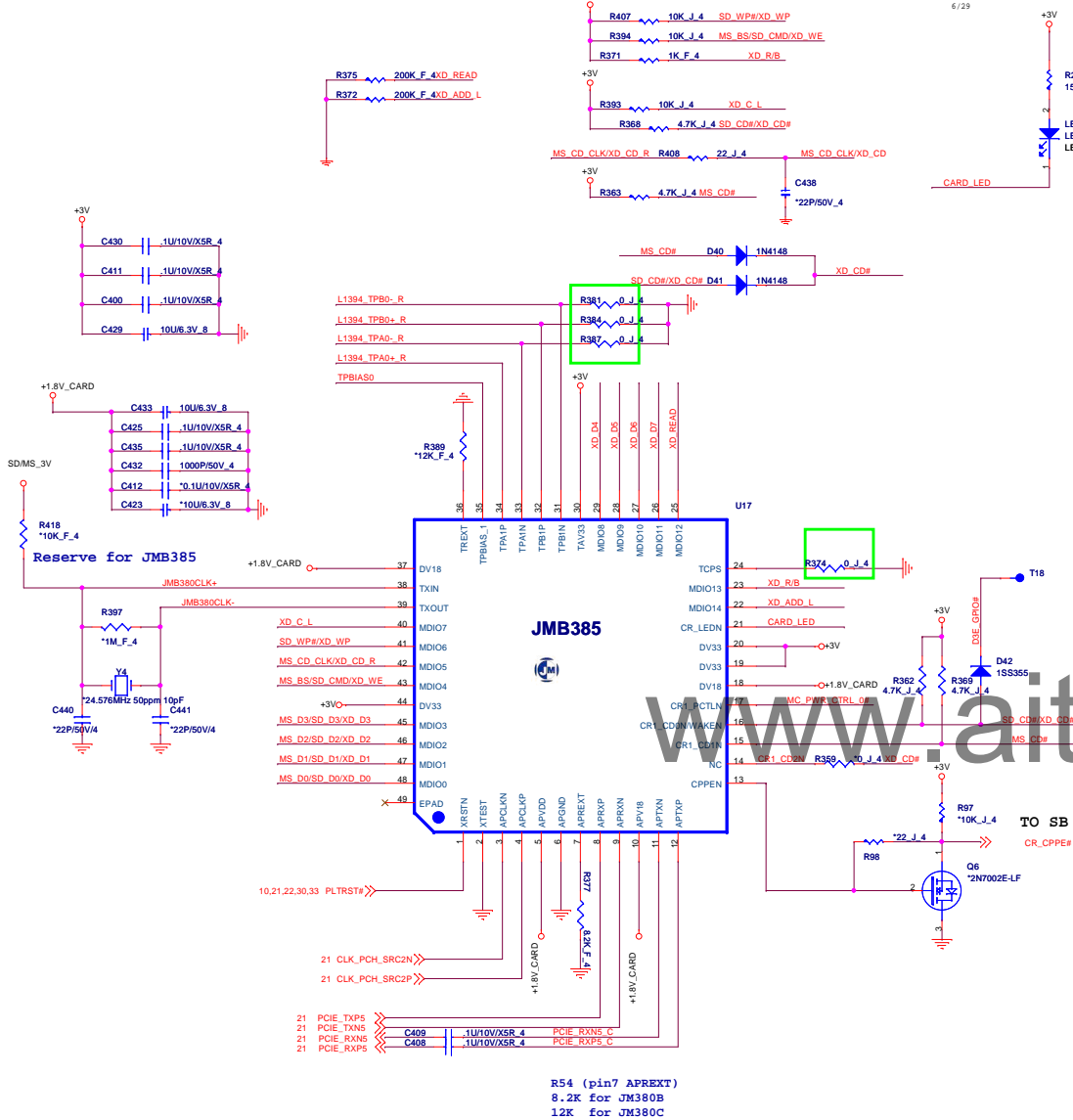


Demodulation Filter

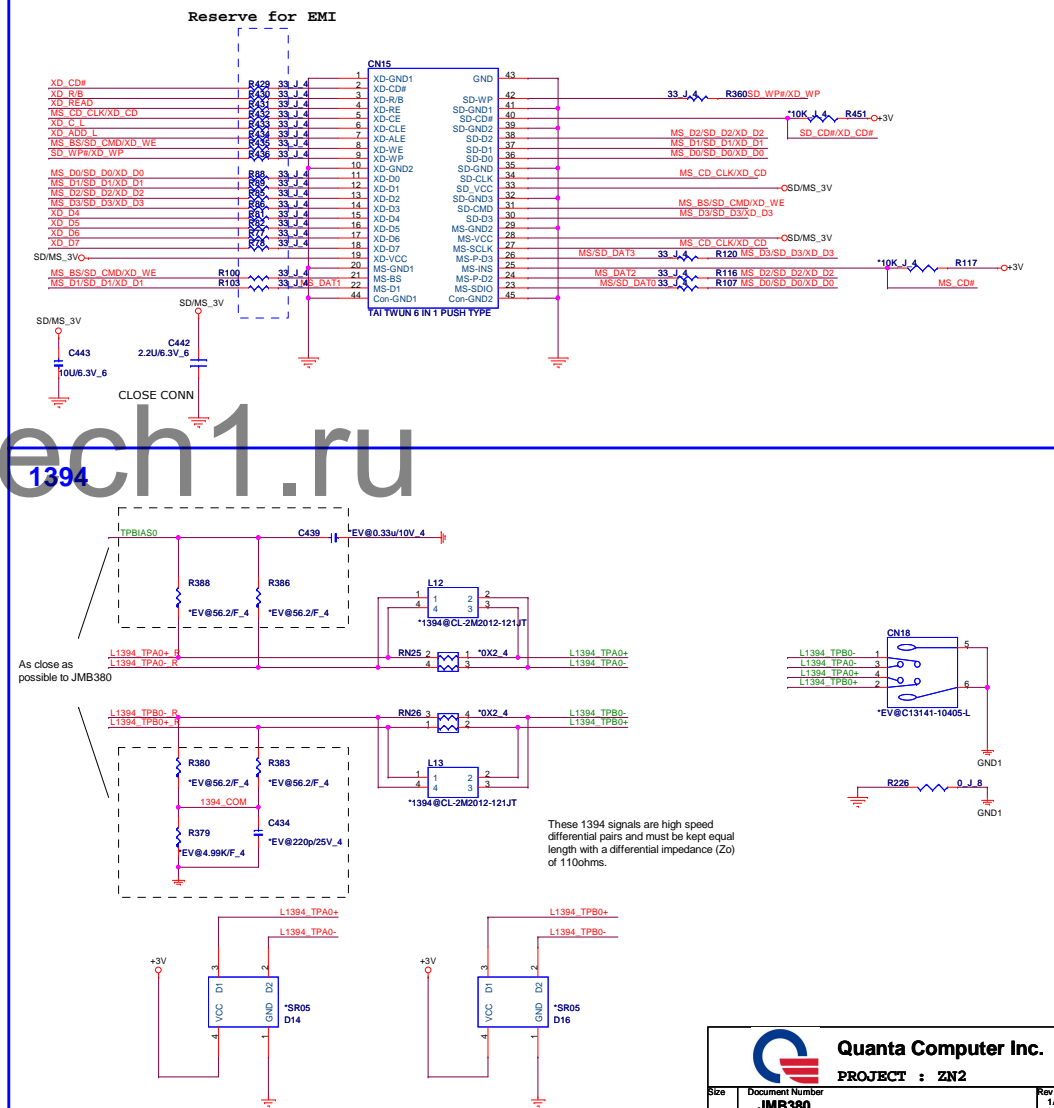
Place close to Codec



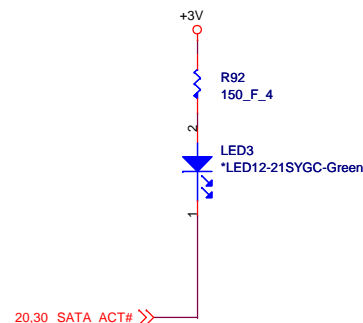




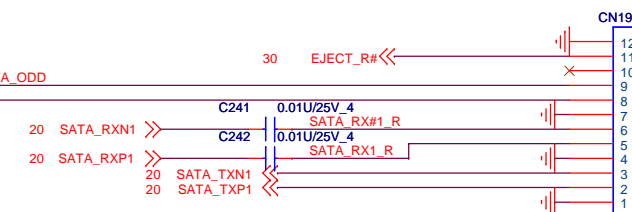
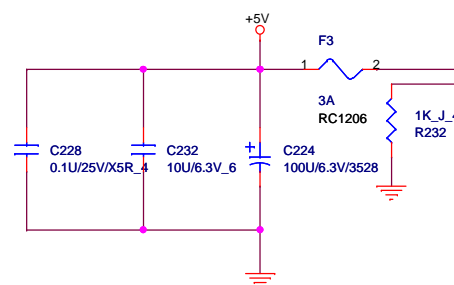
6 IN 1 CONN



SATA HDD CONNECT

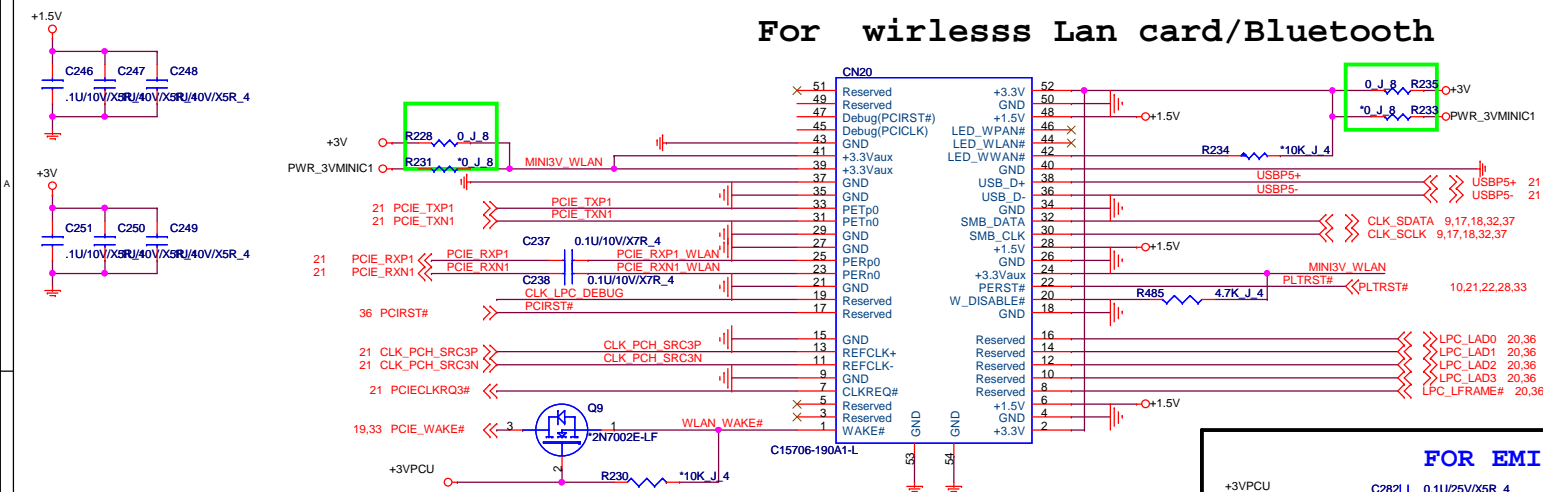


ODD CONN

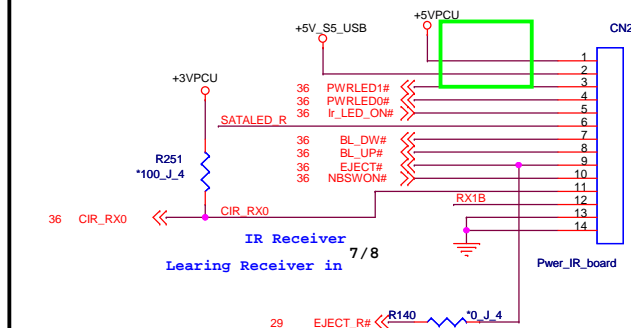


Size	Document Number SATA HDD/ODD	Rev 1A
Date:	Tuesday, March 16, 2010	Sheet 29 of 49

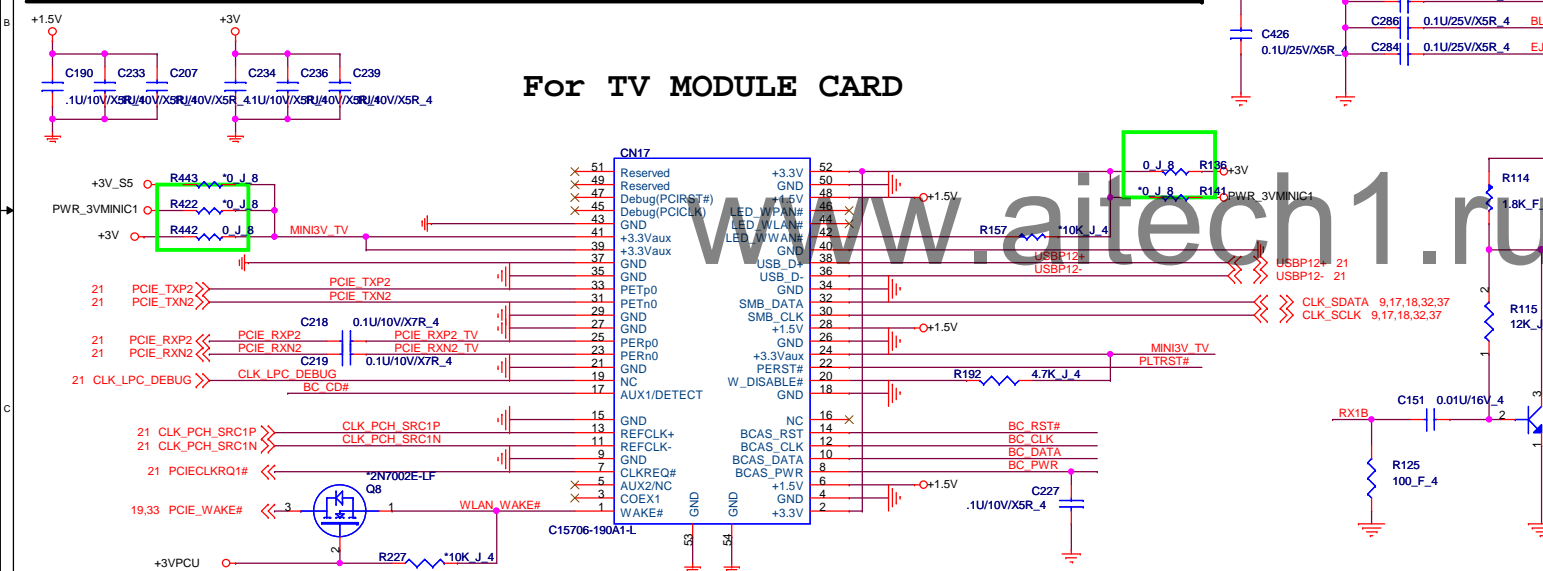
For wirlesss Lan card/Bluetooth



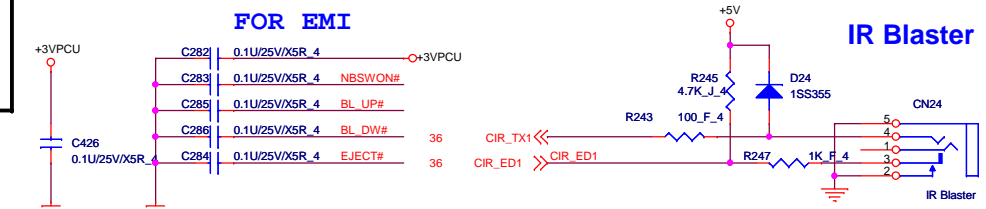
TO POWER BUTTON & LED LIGHT& IR



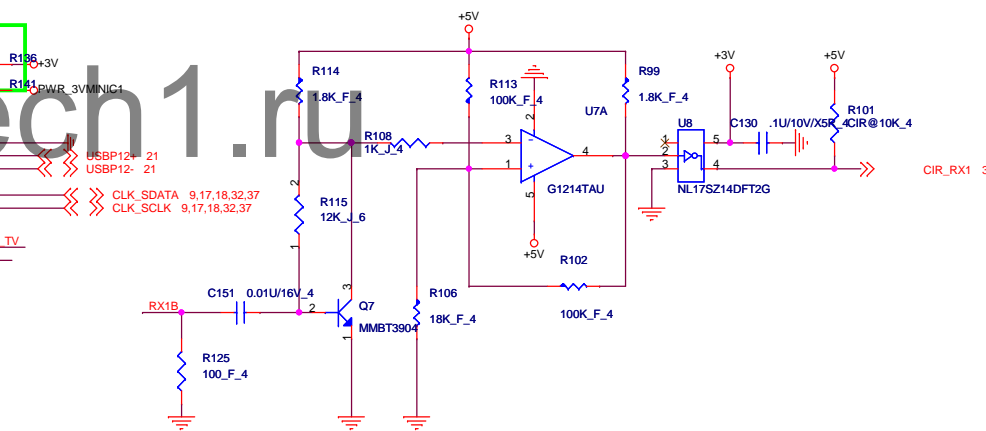
For TV MODULE CARD



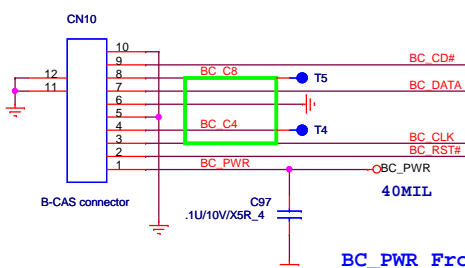
FOR EMI



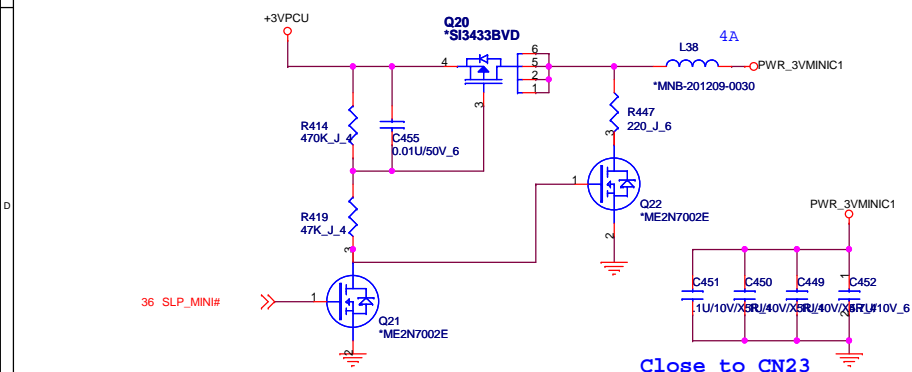
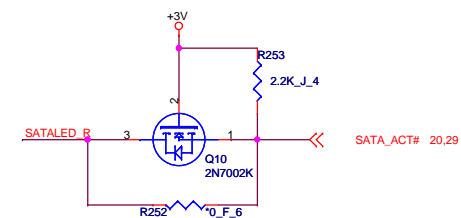
IR Blaster



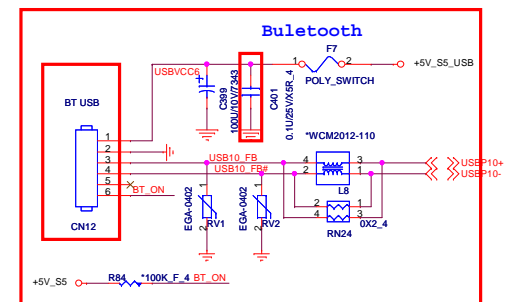
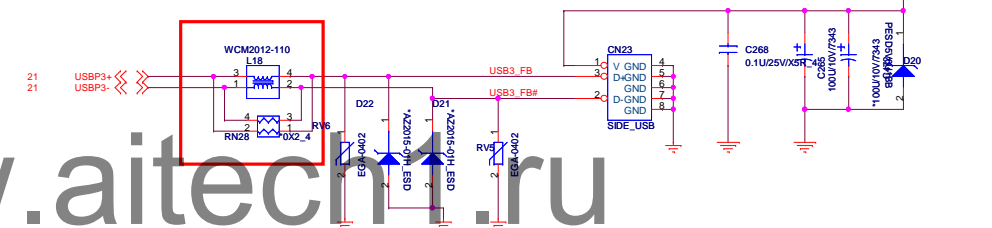
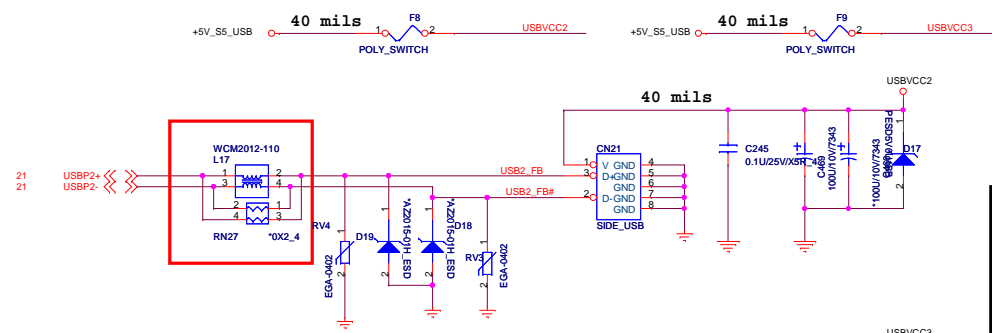
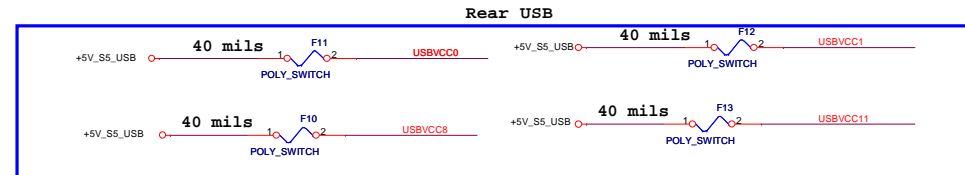
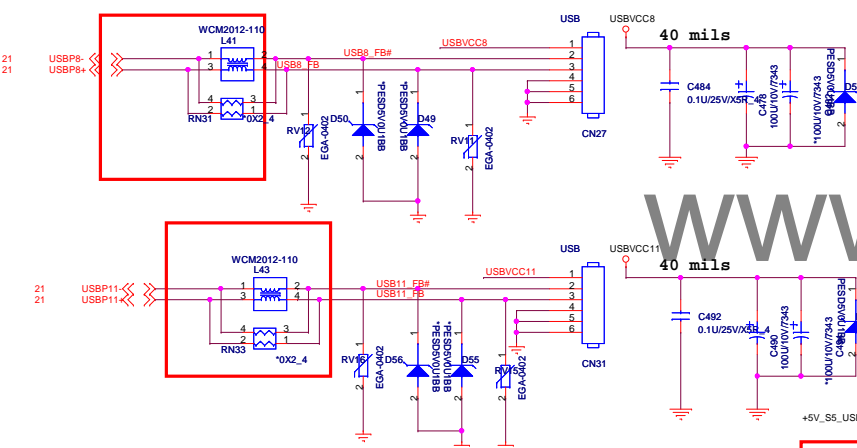
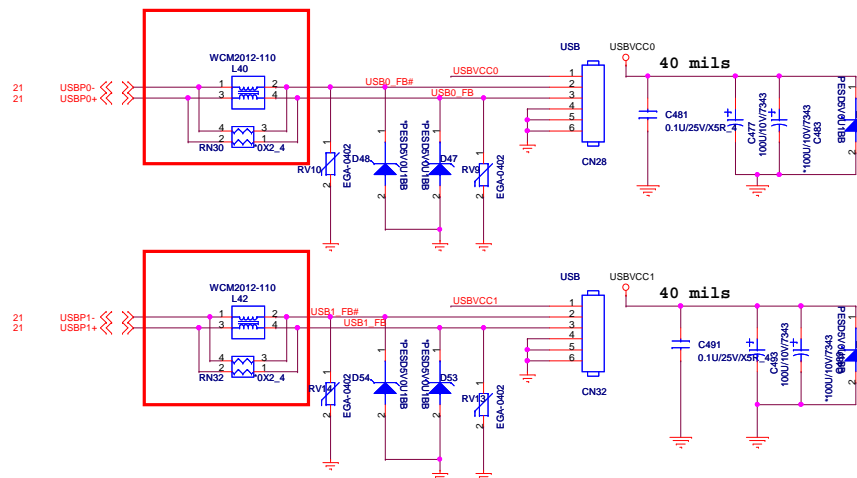
B-CAS CONN



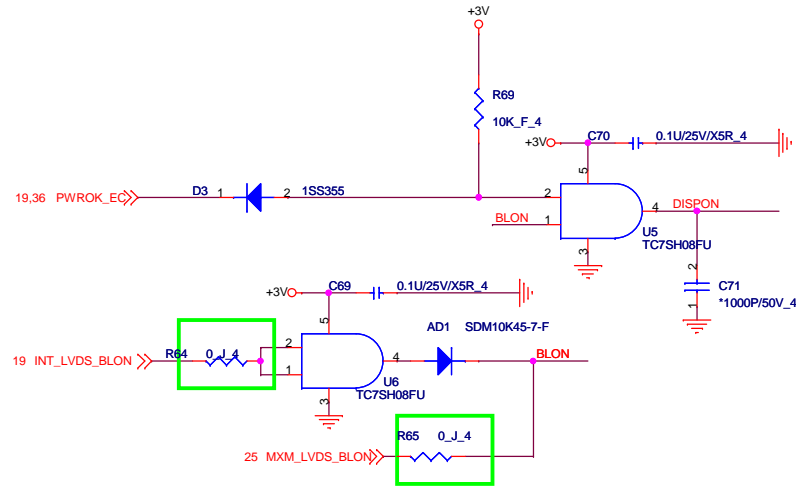
BC_PWR From TV card



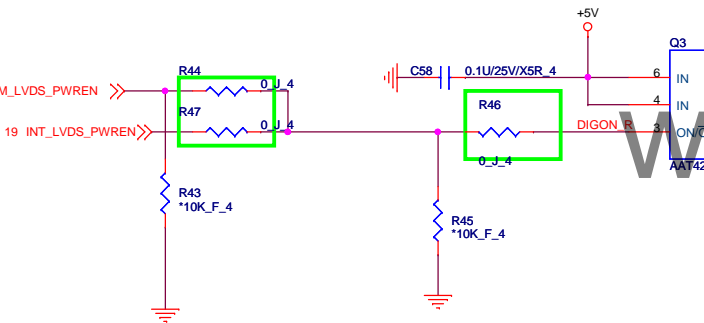
Close to CN23



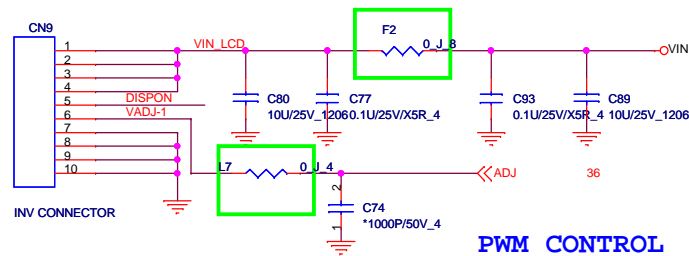
BACKLIGHT CONTROL



PANEL VCC CONTROL

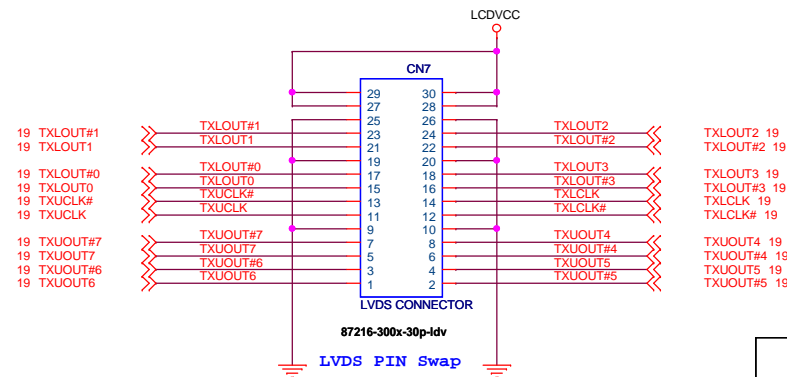


TO INVERTER CONNECT



PWM CONTROL

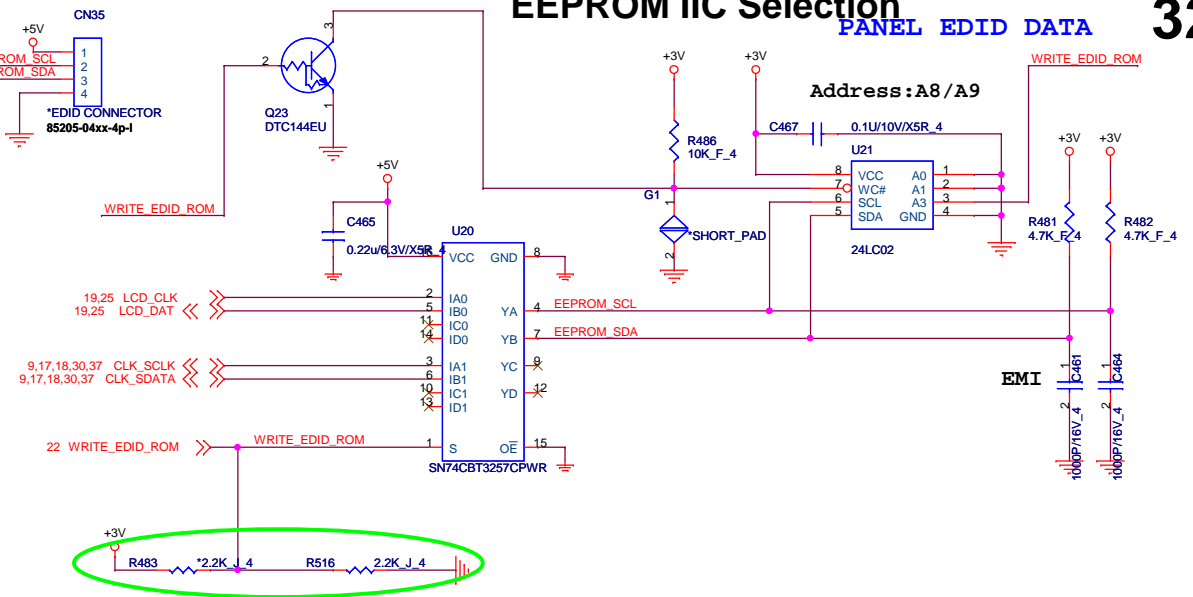
LCD PANEL CONNECTOR



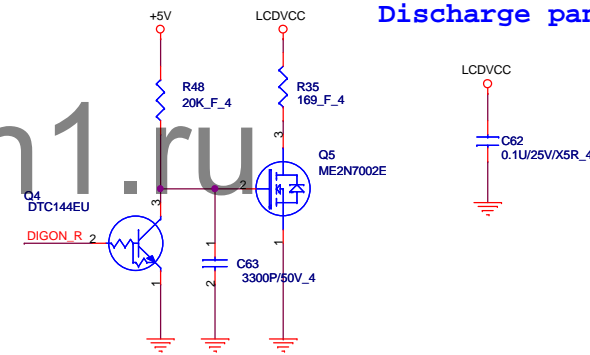
EEPROM IIC Selection

PANEL EDID DATA

32

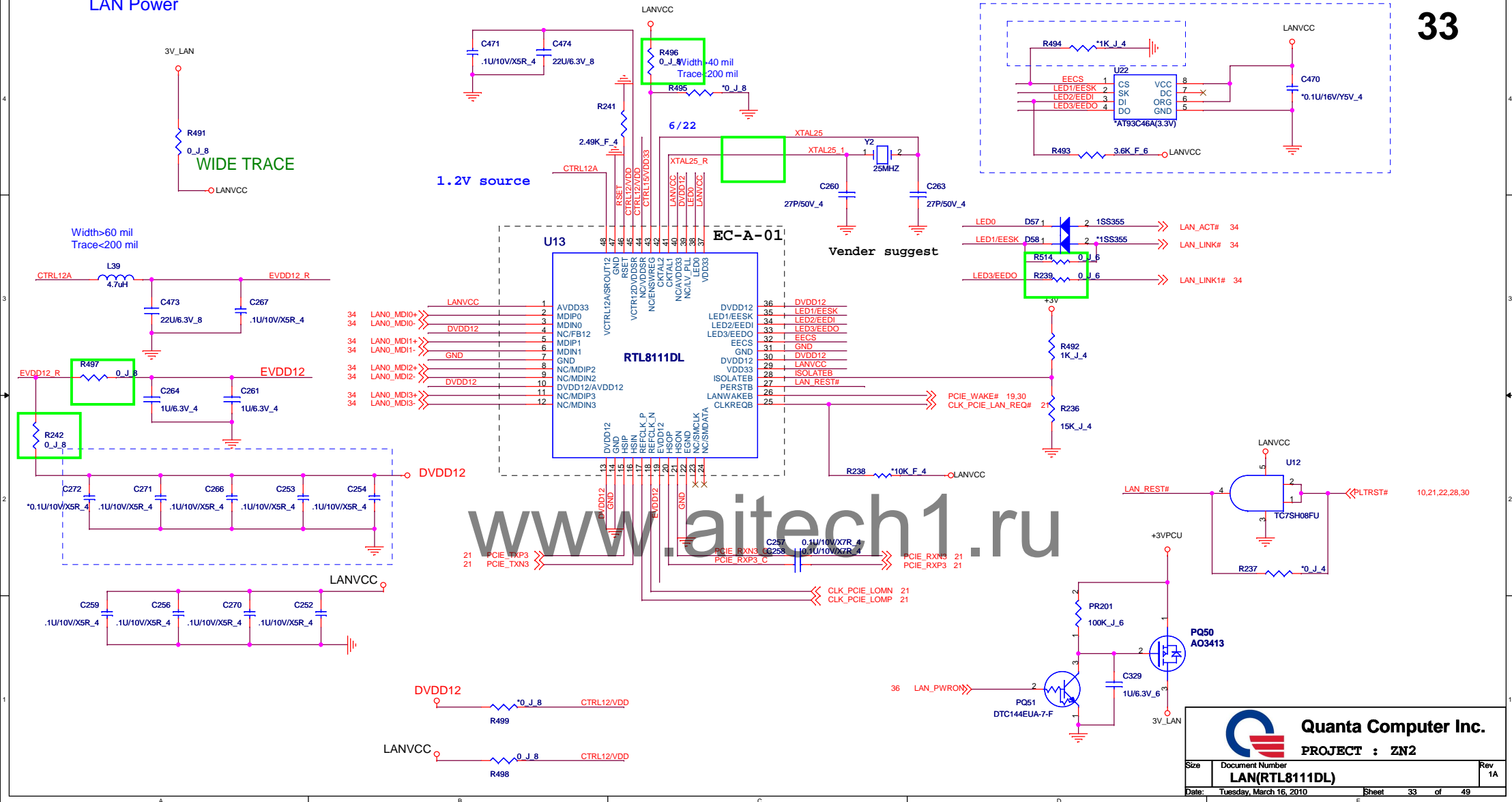


Discharge panel power

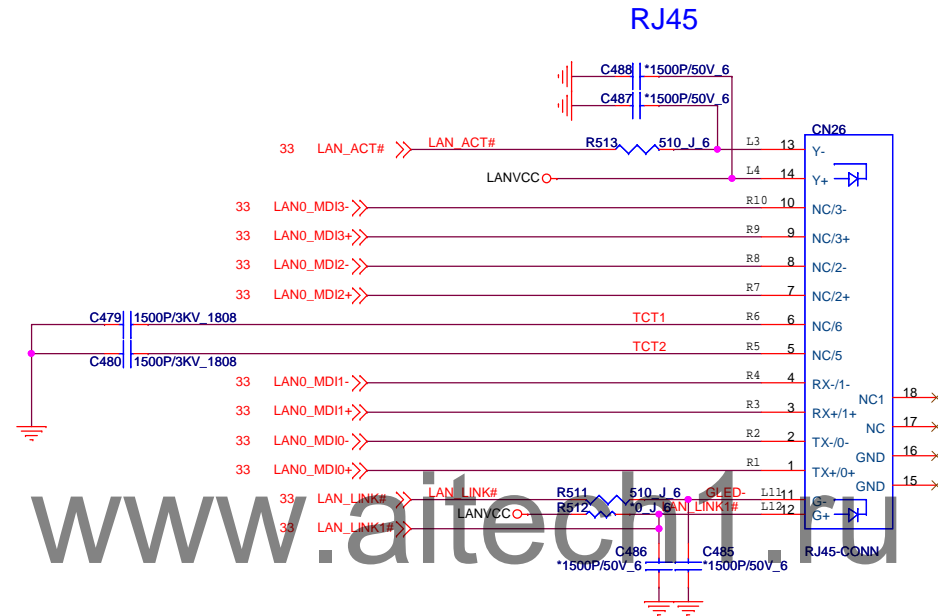


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PROJECT : ZN2



LAN Transformer & EOS CONN to RJ45



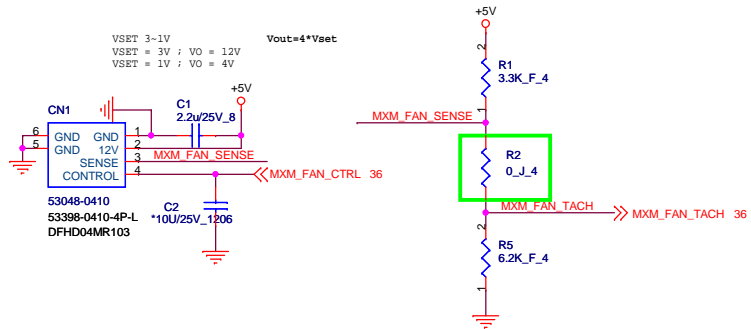
Quanta Computer Inc.

PROJECT : ZN2

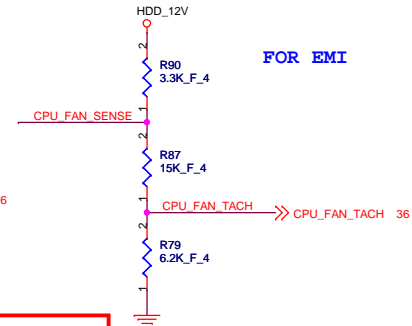
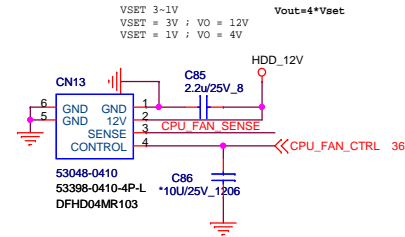
Size	Document Number	Rev
	LAN Transformer & RJ45	1A

Date: Tuesday, March 16, 2010 Sheet 34 of 49

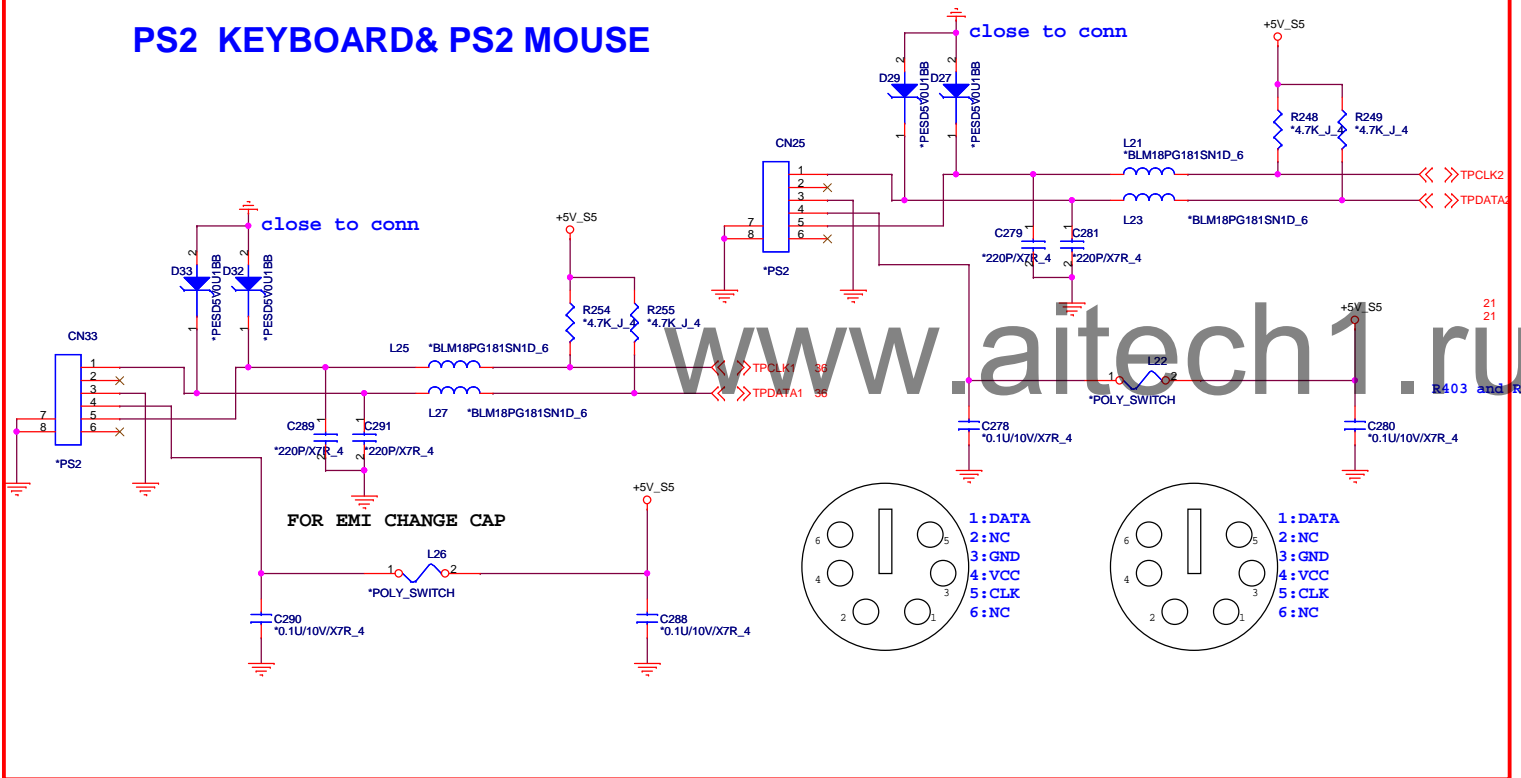
2nd FAN CONN



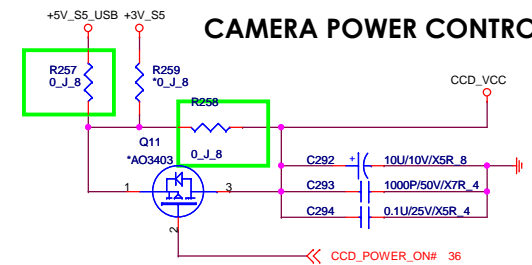
SYSTEM FAN CONN



PS2 KEYBOARD& PS2 MOUSE



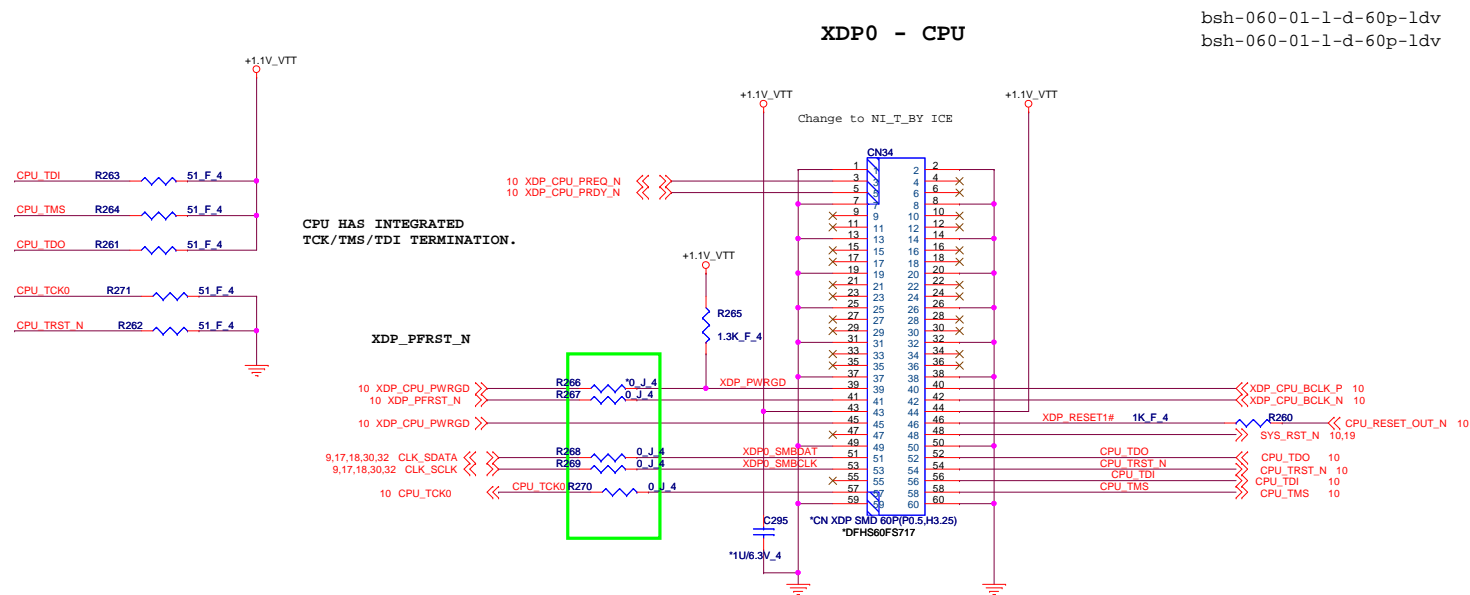
CAMERA POWER CONTROL



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PROJECT : ZN2

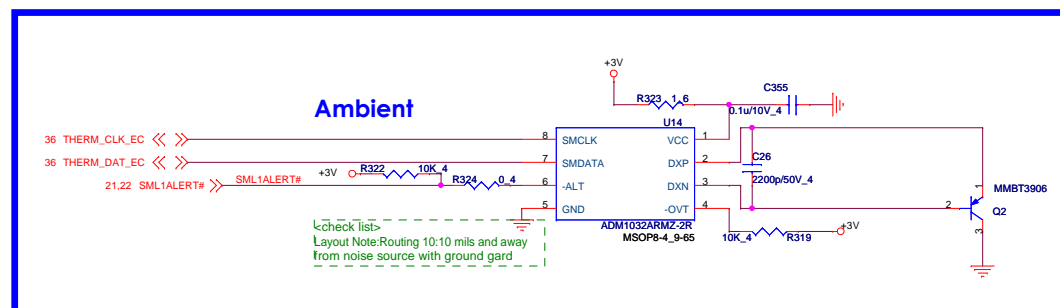
Size	Document Number	Rev
	FAN/Webcam/PS2	A
Date:	Tuesday, March 16, 2010	Sheet 35 of 49

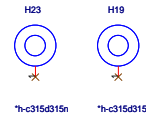
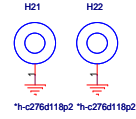
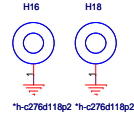
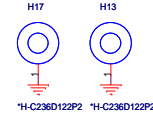
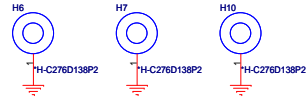
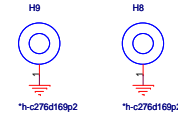


CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

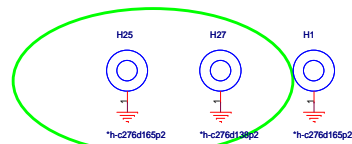
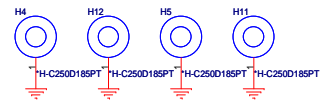
www.aitech1.ru

PCH XDP Connector

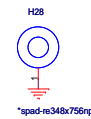


Coaxil conn**WLAN****TV****MXM****CPU frame****CPU fan****Board screw holes**

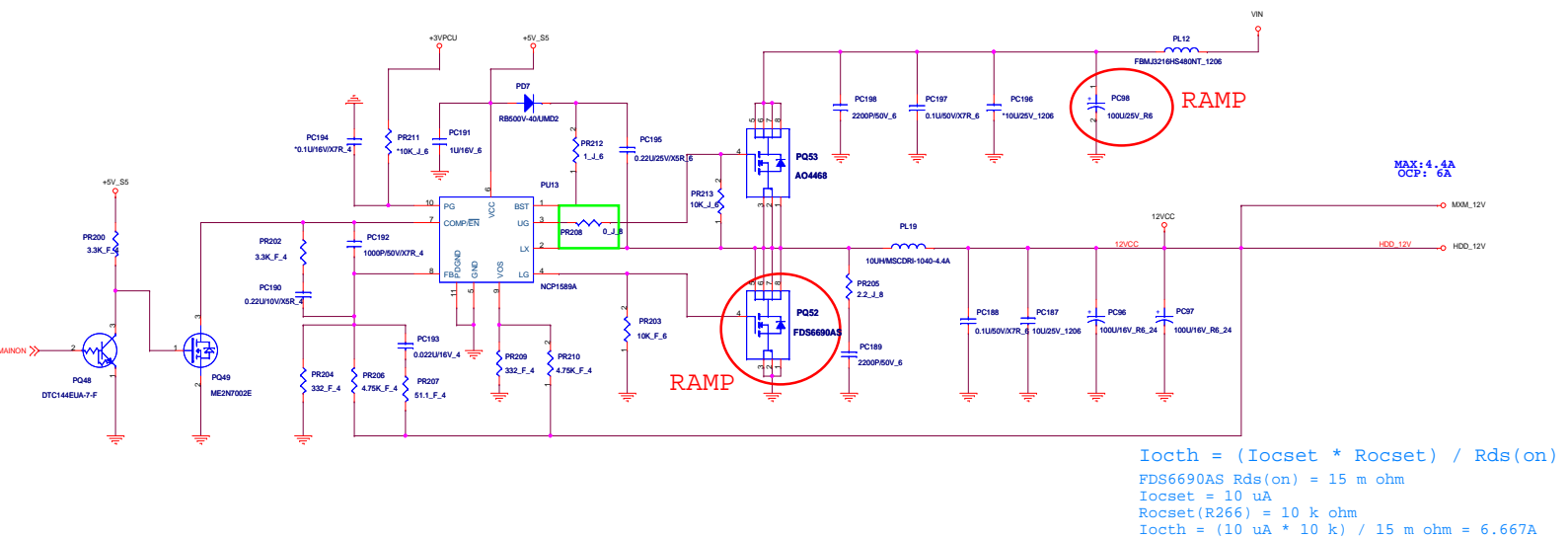
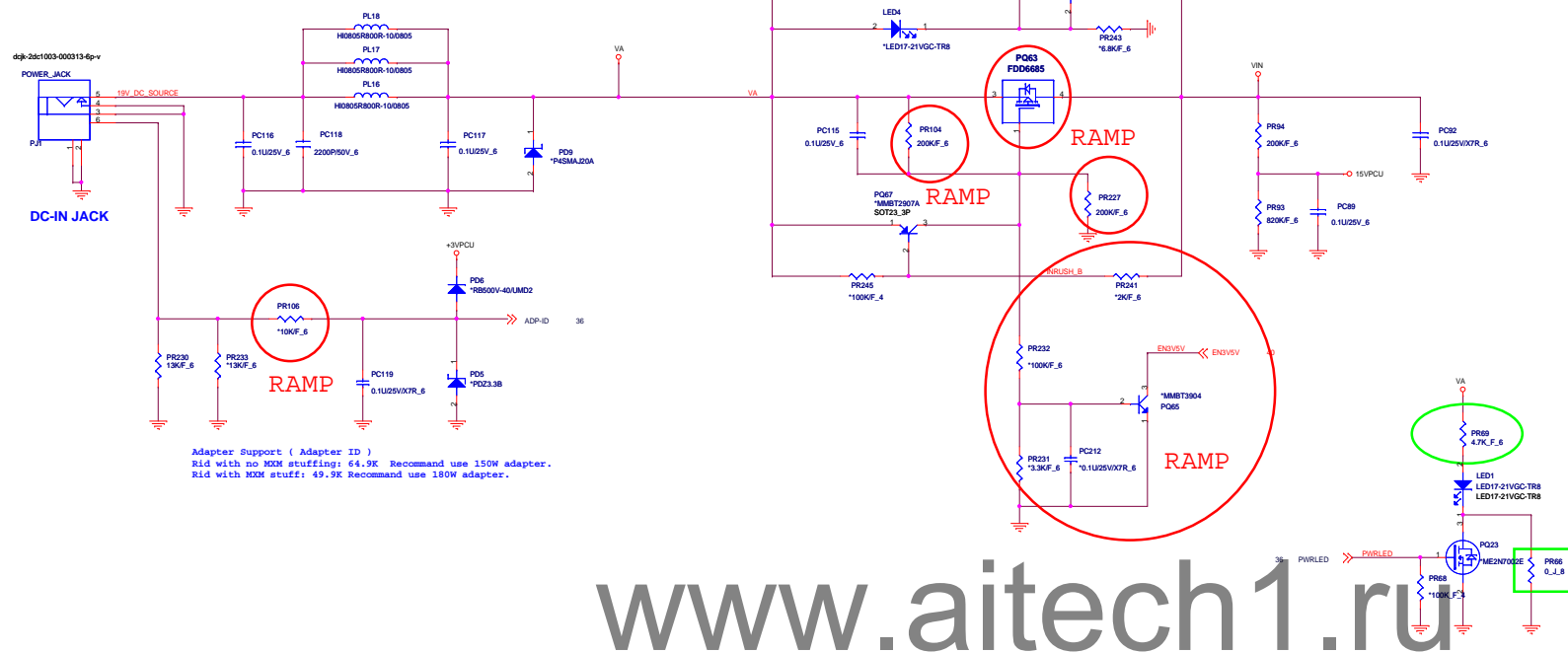
www.aitech1.ru

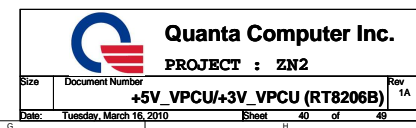
GND SHAPE for EMI in DDR3**CPU socket**

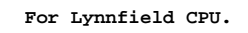
Delete

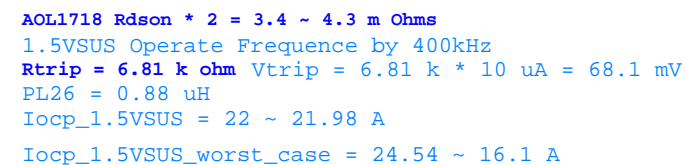


Need discuss with ME/EMI





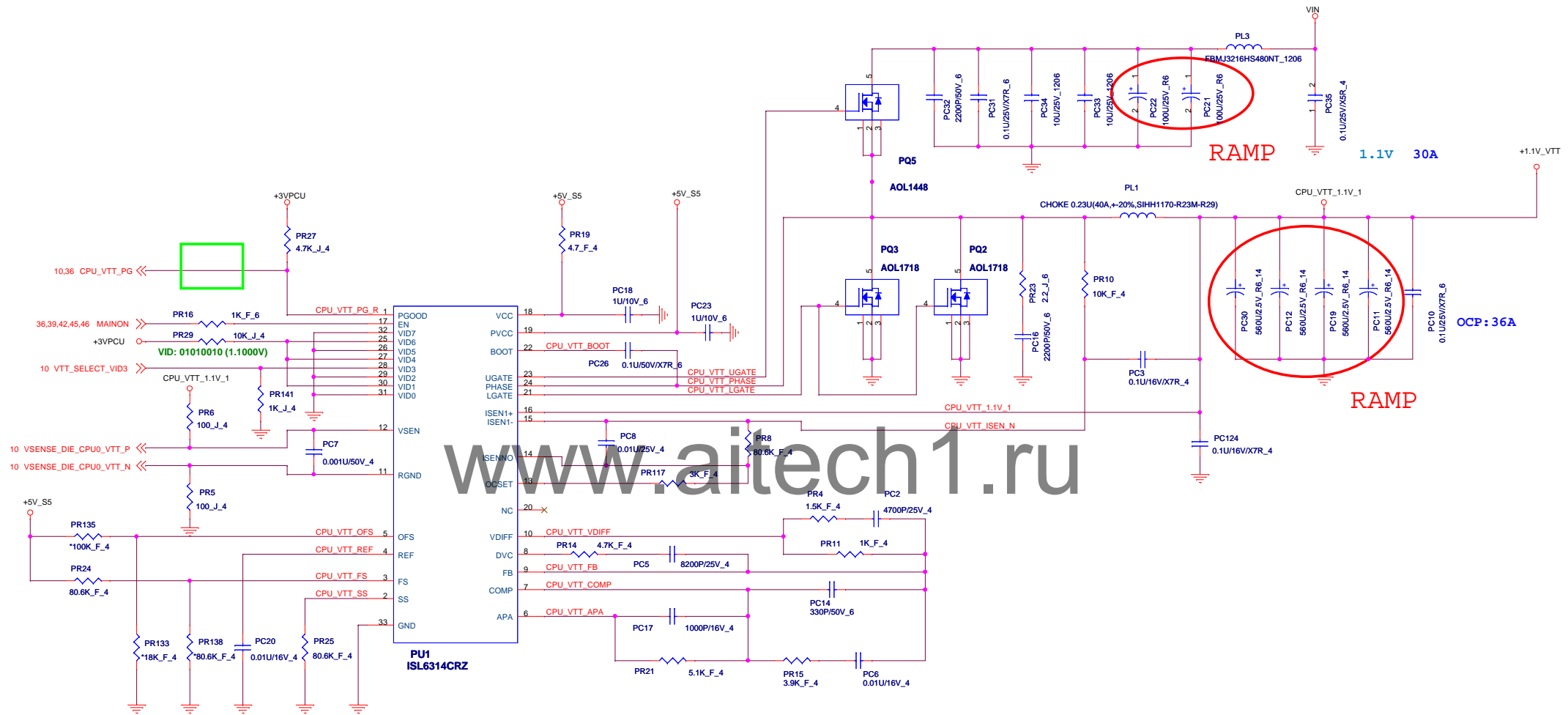


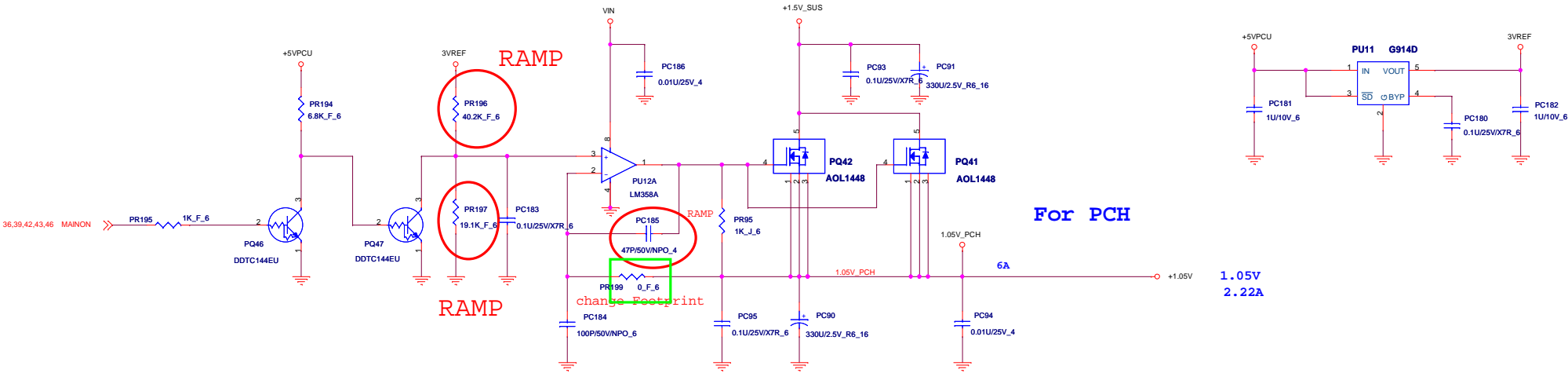


$$I_{ocp} = (V_{trip} / R_{ds_on}) + (I_{ripple} / 2) = (V_{trip}/R_{ds_on}) + (1/(2 * L * f)) * (V_{in} - V_{out})*V_{out} / V_{in}$$

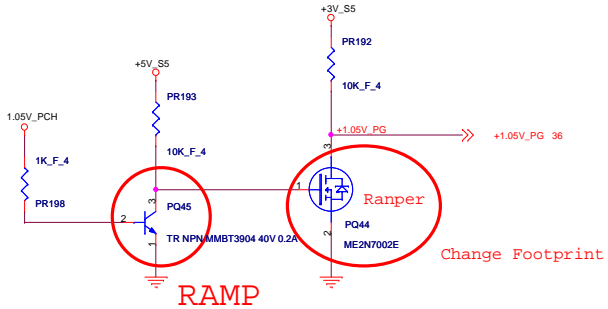
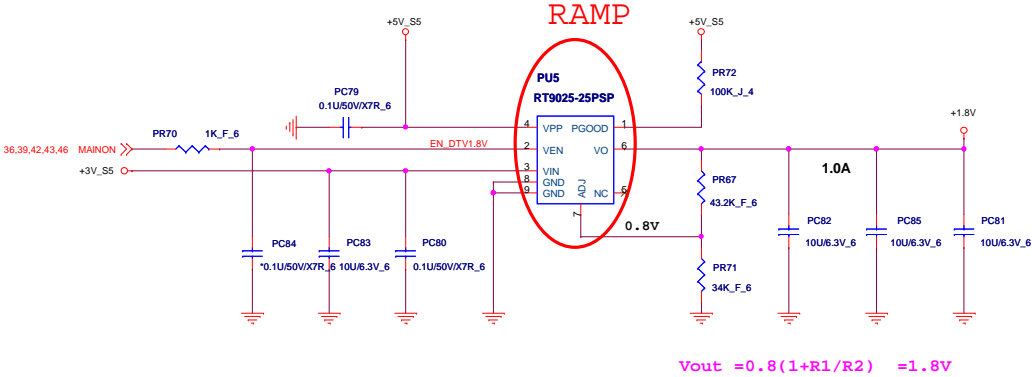
CPU_VTT(1.1V)

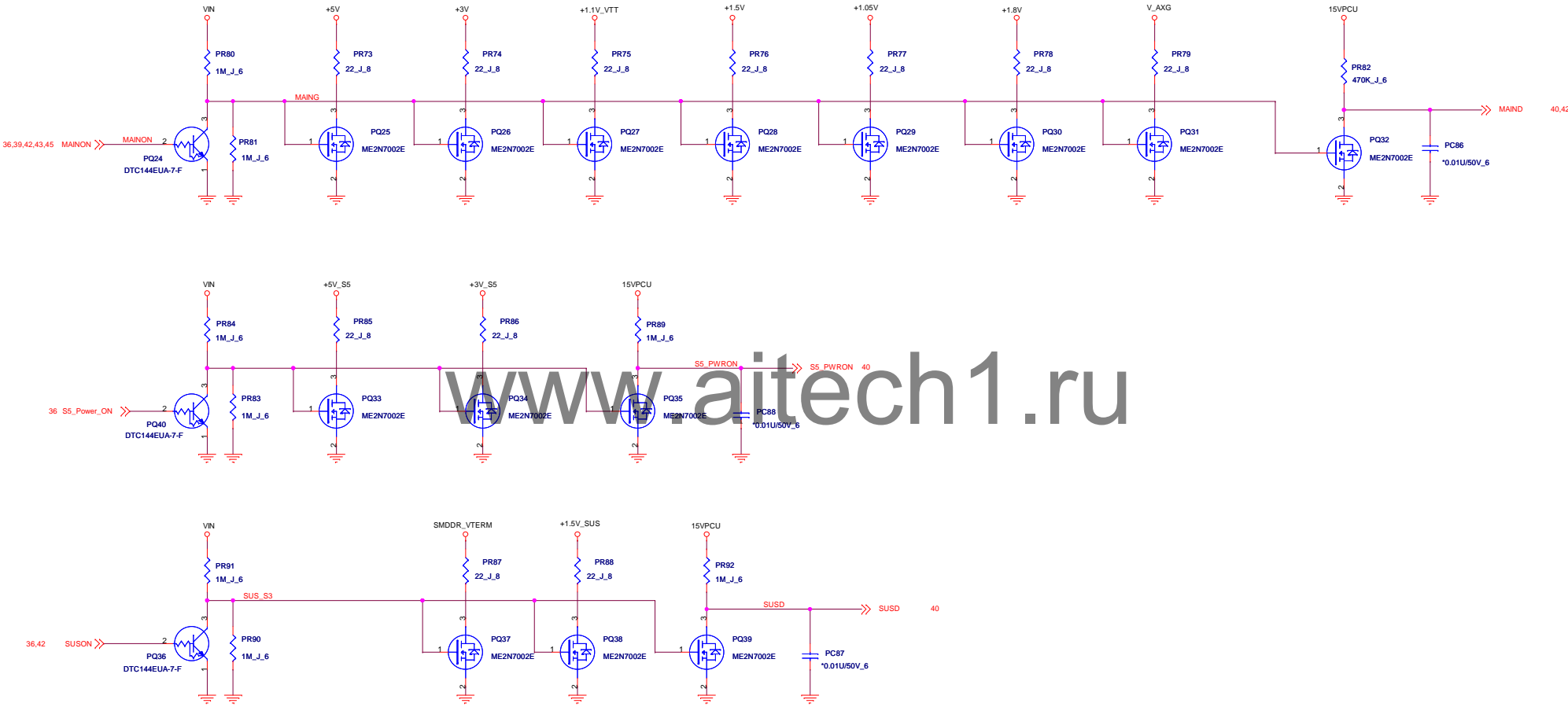
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DATE	ZN2 Schematic file	ZN2 Board file	Revision
DATE	Schematic Change Description		
10.Oct.2009	1. Add +3V pull up trace to CPU_SEL (page 09)		
10.Oct.2009	2. Add the VTT_Select circuit as EL5 does. (page 10)		
10.Oct.2009	3. Change the off page symbol of FDI Sync and Int as output from PCH to Processor. (Page 19)		
10.Oct.2009	4. Populate the series resistance with ICH_PWRBTN# to EC. (Page 19)		
10.Oct.2009	5. Add the CLKRUN# net from EC to ICH. (Page 36)		
10.Oct.2009	6. Change the off page symbol of PMSYNC as the output type from PCH. (Page 19)		
10.Oct.2009	7. Add the test point for L_BKLTCTL (Page 19)		
10.Oct.2009	8. Correct the connection of the following net names: PWROK_EC, MXM_LVDS_BLON, MXM_LVDS_PWREN, (Page 32)		
10.Oct.2009	9. Correct the connection of LCD_CLK and LCD_DAT. (Page 19)		
10.Oct.2009	10. Remove the nets of CRT function and HDMI audio on MXM (Page 25)		
11.Oct.2009	11. Remove the redudant enable for unused port and add the switch IC for DP dual mode. (Page 19)		
11.Oct.2009	12. Add the capacitors for SATA transmitior. (Page 20)		
11.Oct.2009	13. Add GPIO WRITE_EDID_ROM for L10 EDID update (Page 22)		
11.Oct.2009	14. Remove the HDMI audio from PCH to MXM (Page 20)		
11.Oct.2009	15. Reserve the GPIO CR_CPPE# of PCH. (Page 22)		
11.Oct.2009	16. Add the function for CLR_BIOS_DATA and CLR_PASSWD. (Page 22)		
11.Oct.2009	17. Correct the symbol of CLR_BIOS_DATA and CLR_PASSWD. (Page 29)		
11.Oct.2009	18. Correct the STAT capacitors of ODD to receiver. (Page 29)		
11.Oct.2009	19. Use 5V_PCU and +5V_S5 to CN21. (Page 30)		
11.Oct.2009	20. Reserve the GPIO control of CCD_POWER_ON#. (Page 36)		
11.Oct.2009	21. Delete CRT debug from MXM. (Page 25)		
12.Oct.2009	22. Correct the power net for 3VPCU and 5VPCU. (Page 30, 26, 27, 36)		
12.Oct.2009	23. Correct the connection of M_A_DQ46 and M_A_DQ47. (Page 17)		
12.Oct.2009	24. Correct the net name to VR_HOT. (Page 10)		
12.Oct.2009	25. Change the net name of USB4_FB and USB4_FB#. (Page 35)		
12.Oct.2009	26. Change the net name of DDR3 VTT to DDR_VTERM. (Page 17, 18) ==> no change~!!!		
12.Oct.2009	27. Reserve the resistnaces for CK0 and CK1 pairs of CHA and CHB. (Page 17, 18)		
12.Oct.2009	28. Change the MXM_12V on MXM page. (Page 25)		
27.Nov.2009	29. Change net VR_ready Pull High(Page 9)		
27.Nov.2009	30. Delete MXM to VGA port circuit(Page 25/27)		
27.Nov.2009	31. Change ACN4 to right angle typy(Page26)		
27.Nov.2009	32. Delete CN16 XDP connect (Page37)		
27.Nov.2009	33. Swap USB2, USB3, USB10, differential signal(Page31)		
27.Nov.2009	34. Delete all JP connection		
27.Nov.2009	35. CN14 LCD_Clk & LCD_Data swap(Page25)		
27.Nov.2009	36. CLK_LPC_DEBUG net change to CN17 pin19(Page30)		
27.Nov.2009	37. PEG_CLKREQ#_R pull low,Change R457 resistor to R454(Page21)		



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	CHANGE LIST	1A
Date	Tuesday, March 16, 2010	Sheet 47 of 49

DATE	ZN2 Schematic file	ZN2 Board file	Revision
DATE	Schematic Change Description		
27.Nov.2009	38. Change ACin Soft start Function and add Adaptor ID to identify Function and disable ID to identify and delete Short Pad JP5, JP6 (Page 39)		
27.Nov.2009	39. Delete Short Pad PJP7, PJP8, PJP9, PJP10, PJP11, PJP12 (Page 40)		
27.Nov.2009	40. Delete short Pad PJP4, PJP5 and Place up PR190 for V_AXG initial setting Voltage Place up PR48 for V_AXG PG Pull high (Page 41)		
27.Nov.2009	41. Change PR116 Value to 6.81K ohm and PL4 Value to 0.88uH and add Location PC210, PC211, PQ64 and delete Short Pad PJP1 (Page 42)		
27.Nov.2009	42. Delete Short Pad PJP2, PJP3 (Page 43)		
27.Nov.2009	43. Change CPU core Value PR132, PR122, PR140, PR145, PR150, PR154 (Page 44)		
27.Nov.2009	44. Delete Short Pad PJP6 (Page 45)		
27.Nov.2009	45. Place up PQ27, PQ28, PQ29, PQ30, PQ31, PQ38, PR88 (Page 46)		
29.Nov.2009	46. MOVE EC circuit (PAGE 36)'s LED indicate circuit to (Page 39) ACin circuit		
2.Dec.2009	47. Connect GFX_VR_EN to dGPU_PRSENT# (Page 10)		
2.Dec.2009	48. Add RC circuit for SRTC_RST# (Page 20)		
2.Dec.2009	49. Change CLK_PCIE_DMI# differential pair RP15 to L44/L45 (Page 21)		
2.Dec.2009	50. Change C328 to 330uF and Delete C329,C335,C336,C343,C344(Page 14)		
2.Dec.2009	51. Remove R174 10Kohm(Page 25)		
2.Dec.2009	52. Remove R389 , place R374 to 0 ohm, 1394 component, Change U17 to UMB385 (Page 28)		
2.Dec.2009	53. Change CN11 to right angle type(Page 29)		
2.Dec.2009	54. Place the SATA_ACT circuit component(Page 30)		
2.Dec.2009	55. Remove the hall sensor component and add LED5(Page 36)		
2.Dec.2009	56. Add SW1 (Page 36)		
7.Dec.2009	57. Reverse HDD connect pin (Page 29)		
26.Jan.2010	58. Change Write_EDID_ROM to GPIO28 (Page 22)		
26.Jan.2010	59. Reserve MXM to CRT function (Page 25/27)		
26.Jan.2010	60. Reserve R395 for PEG_CLKREQ pull high (Page 25)		
26.Jan.2010	61. Change C274/C276 to 47u (Page 27)		
26.Jan.2010	62. Change CN29 Pin2 power to +5V_S5_USB (Page 30)		
26.Jan.2010	63. Change F7/F8/F9 power to +5V_S5_USB (Page 31)		
26.Jan.2010	64. Change C447,C483,C493,C489,C478,C482,C490,C494,,C287,C399,C265,C472,C469,C466 to 100u/7343 type (Page 31)		
26.Jan.2010	65. Add D61 (Page 31)		
26.Jan.2010	66. Reserve R232 for Write_EDID_ROM pull low function (Page 32)		
26.Jan.2010	67. Add C329 for Lan loss solution (Page 33)		
26.Jan.2010	68. CN29 Pin15/16 floating (Page 34)		
26.Jan.2010	69. Change R257 power to +5V_S5_USB (Page 35)		
26.Jan.2010	70. Reserve R63 (Page 36)		
26.Jan.2010	71. Add ADP-ID to EC ADC1 (Page 36/39)		
26.Jan.2010	72. Change Screw H23,H19,H2,H4,H5,H11,H28 (Page 38)		
26.Jan.2010	73. Change ACin Adaptor ID to identify Function circuit and add delay time for EN3V5V enable circuit(Page 39)		

Size

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CHANGE LIST

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1A

 **Quanta Computer Inc.**
PROJECT : ZN2

4. Nat name Description :

Voltage Rails

VIN	Primary DC system power supply
+5VPCU	5.0V always on power rail by LATCH or ACIN
+3VPCU	3.3V always on power rail by LATCH or ACIN
+5V_S5	5.0V always on power rail by DCON
+3V_S5	3.3V always on power rail by DCON
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+5V_S5_USB	5.0V power rail by SUSD
+3V	3.3V switched power rail by MAIND
+5V	5.0V switched power rail by MAIND
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+VCC_CORE	Core Voltage for CPU
CPU_VTT_1.1V	1.1V power rail for AGTL+ termination/Core for GMCH by MAINON
1.05V_PCH	1.05V power rail for PCH Core Power by MAINON
+1.8V	1.8V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for VRM/NVRAM by MAINON
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+1.5V	1.5V power rail for MiniPCI by MAIND
+1.5V_SUS	1.5V power rail for DDRIII by SUSON
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SMDDR_VTERM	0.75V DDRIII Termination Voltage by MAINON

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Normal Signal / Ground 1 Plane
Layer 5		Power Plane
Layer 6		Solder Side, Microstrip signal Layer

Layers : 6 Depth 1.6mm Impence 55 ohms +/- 10%

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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